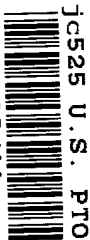


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# UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. 6136/53461

First Inventor or Application Identifier Tetsuzo Yoshimura, et al.

Title "MULTI-LAYER OPTO-ELECTRONIC SUBSTRATES WITH..."

Express Mail Label No. TB80693315X US

## APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ \* Fee Transmittal Form (e.g., PTO/SB/17)  
(Submit an original and a duplicate for fee processing)
2. ☒ Specification [Total Pages 98]  
(preferred arrangement set forth below)
  - Descriptive title of the Invention
  - Cross References to Related Applications
  - Statement Regarding Fed sponsored R & D
  - Reference to Microfiche Appendix
  - Background of the Invention
  - Brief Summary of the Invention
  - Brief Description of the Drawings (if filed)
  - Detailed Description
  - Claim(s)
  - Abstract of the Disclosure
3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 62]
4. Oath or Declaration [Total Pages 5]
  - a. ☒ Newly executed (original or copy)
  - b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))  
(for continuation/divisional with Box 16 completed)
    - i. ☐ DELETION OF INVENTOR(S)  
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

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5. ☐ Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
  - a. ☐ Computer Readable Copy
  - b. ☐ Paper Copy (identical to computer readable copy)
  - c. ☐ Statement verifying identity of above copies

## ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement of Power of Attorney (when there is an assignee)
9. ☐ English Translation Document (if applicable)
10. ☐ Information Disclosure Statement (IDS)/PTO-1449
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)  
(Should be specifically itemized)
13. ☐ \* Small Entity Statement(s) filed in prior application, Status still proper and desired (PTO/SB/09-12)
14. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
15. ☒ Other: COMMUNICATION

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:
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**MULTI-LAYER OPTO-ELECTRONIC SUBSTRATES WITH ELECTRICAL AND  
OPTICAL INTERCONNECTIONS AND METHODS FOR MAKING**

**CROSS-REFERENCE TO RELATED APPLICATIONS**

5           This application claims the benefit of US Provisional Application 60/103,726  
filed October 9, 1998.

**FIELD OF THE INVENTION**

10           The present invention relates to opto-electronic substrates that may be used to  
connection digital and/or analog electronic systems, and methods for making such  
systems. More specifically, the present invention relates to opto-electronic substrates that  
have both electrical and optical interconnections, and methods for making such  
substrates. The present invention may be applied to multichip modules (MCMs) and the  
like.

**BACKGROUND OF THE INVENTION**

15           With the increase in clock rates and I/O counts of processing systems  
implemented on interconnection substrates, the problems of interconnection bottlenecks,  
noise, signal attenuation, heat generation, and maintaining synchronizable connection  
20   lengths in the electrical connections of such systems are appearing. An optical  
interconnect has the advantage of low RC delay, low signal attenuation, predictable  
delay, low power, low noise and high tolerance to opens and shorts. However, there is a  
large barrier which prevent optical interconnections from being used in high-speed  
digital/analog systems. Thus far, bulky driver chips and amplifier chips have been  
25   required to provide the conversions between the optical signals in the optical  
interconnects and the electrical signals which are generated and used by the electronic  
chips. Each electrical signal that is to be convey optically over a long distance requires a  
light emitting device, a driver chip to generate the electrical power for switching the  
light-emitting device at one end of the optical connection. At the receiving end of the

optical connection, a photo-detector device and an amplifier is required to convert the optical signal to electrical form. The amplifier is needed because the light power becomes small at the photo-detector device due to considerable loss in conventional optical paths. The driver and amplifier components require space on the circuit substrate, and therefore represent barriers to using large numbers of optical connections in a substrate, like a multichip module. In fact, the area needs of these components, as well as the area needs for the emitter devices and photo-detector devices, would increase the size of the module substrates to be larger than module substrates with pure electrical connections. These excess components and their assembling increase manufacturing costs. Furthermore, the conventional optical connections have longer delay due to EO and OE conversions, which would not provide significant speed benefits over pure electrical modules.

The present application is directed to providing optical connection configurations and methods for manufacturing the optical connections such that the above problems may be overcome.

### **SUMMARY OF THE INVENTION**

One aspect of the present invention eliminates the need for the bulky drivers and amplifiers, which significantly reduces area requirements. In the place of a light-emitting source, the combination of an external light-source and an optical switch device (e.g., modulator) is used. The optical switch device is responsive to an output of an IC chip, and does not required a driver chip for operation. In contrast to light emitting source cases, the power of optical signals in implementations using light modulators can be greatly increased by increasing the size and power of the external light source. The external light source can be easily increased in this manner since it does not need to be modulated. For example, it can be implemented as a simple continuous wave (CW) or pulse trains source of optical power. In addition, losses in the optical connection are reduced. Therefore, and power at the photo-detectors is increased, which enables the amplifiers to be eliminated. The losses are reduced by integrally forming polymeric waveguides with the optical switches and the photo-detectors, which increases optical

coupling efficiency. Additionally, the construction methods of the present invention enable short optical connections to be made. Optical power to the photo-detector device is increased by using the external optical power. In addition, optical waveguide integration methods of the present invention enable highly efficient optical connections to be made to VCSEL and laser-diode (LD) emitter devices, which enables these devices to be used as sources of optical power in addition to external sources.

Another aspect of the present invention realizes device and/or material integration into an "opto-electronic (OE) layer", which increases room for chip-mounting, and reduces the total system cost by eliminating the difficulty of optical alignment between OE devices and optical waveguides. OE devices can be embedded into waveguide layers by using wafer processing techniques according to the present invention. Methods according to the present invention enable opto-electronic devices (e.g., modulators, VCSELs, photo-detectors, optical switches, laser-diode(LD), driver chips, amplifier chips, *etc.*) to be integrated with optical waveguides in ultra thin polymer layers on the order of 1  $\mu\text{m}$  to 250  $\mu\text{m}$ .

Another aspect of the present invention provides OE substrates by stacking the above-described OE layers on top of one another and by joining them together, such as by lamination or by a build-up fabrication process. The OE layers can then be overlaid upon the surface of a conventional electrical substrate without requiring extra room for the photo-detectors, optical-switches, light-emitting components, driver chips, amplifier chips, *etc.* In fact, multiple OE layers can be stacked upon one another to provide all the required photo-detectors optical-switches, light-emitting devices, driver chips, amplifier chips, *etc.* The present application provides several construction methods for forming these OE layers, and also provides several substrate configurations.

Another aspect of the present invention is a method to stack two or more OE films, permitting an increase in the functionality of the stacked structure compared to a single OE film. Each OE film may comprise a single-layer structure or be build-up-of multiple-layer structures, including electrical layers by a Z connection method. The OE layers and electrical layers on each OE film may be optimized separately. Preferred



embodiments of stacked OE films include flexible interconnections, OE Interposers, film OE-MCM, both-side packaging, back-side connection, and a Film Optical Link Module (FOLM). Additionally, stacked films permit the use of a greater variety of fabrication processes compared to a single film. In particular, a stacked film enables both-side processing by permitting processed layers to be inverted upside-down.

These features provide the advantageous effect of enabling large-scale optical interconnections to be added to electrical substrates without increasing area requires of the substrate. These features also enable the optical coupling efficiencies of optical interconnections to be increased. These features are also applicable to optical-parallel-link modules.

In the present application, examples of multichip modules are principally shown. However, the same features and aspects of the present invention are applicable to electrical backplanes, printed-circuit boards (PCBs), chip size packages (CSPs), and other substrates.

### **DESCRIPTION OF DRAWINGS**

FIG. 1 is a first embodiment of an optical-electrical multichip-module substrate according to the present invention.

FIGS. 2 and 3 are a first embodiment of an optical switch according to the present invention.

FIGS. 4-1 and 5-1 are a first embodiment of a photo-detector device according to the present invention.

FIGS. 4-2 and 5-2 are a second embodiment of a photo-detector device according to the present invention.

FIGS. 4-3 and 5-3 are a third embodiment of a photo-detector device according to the present invention.

FIG. 6 is a second embodiment of an optical-electrical multichip-module substrate according to the present invention.

FIGS. 7 and 8 are a first embodiment of a lateral emitter device according to the

present invention.

FIG. 9 and 10 a first embodiment of a vertical emitter device according to the present invention.

FIG. 11-20 illustrate construction methods according to the present invention.

5 FIGS. 21-26 are views of a first multichip module system according to the present invention.

FIGS. 27-30 illustrate construction methods for making selected components used in the system of FIGS. 21-26 and other systems according to the present invention.

10 FIGS. 31, 32, and 32-1 are views of a second multichip module system according to the present invention.

FIGS. 33-36, and 37-1 through 37-4 illustrate further embodiments of the optical-electrical multichip-module substrates according to the present invention.

FIGS. 38-68 illustrate further construction methods for the optical-electrical multichip-module substrates according to the present invention.

15 FIGS. 69-70 illustrate a free-space MCM system according to the present invention.

FIGS. 71-73 illustrate three-dimensional MCM systems according to the present invention.

20 FIGS. 74-81 show schematic views of an exemplary thin film with integral devices and waveguides as being fabricated according to another process according to the present inventions.

FIGS. 82-89 show schematic views of another exemplary thin film with integral devices and waveguides as being fabricated according to another process according to the present inventions.

25 FIGS. 90-104 show perspective views of an exemplary waveguide layer being processed according to exemplary methods for forming vertical and horizontal optical couplers according to the present invention.

FIGS. 105 and 106 are top plan and cross-sectional views, respectively, of an exemplary corner turning mirror according to the present inventions.

FIGS. 107 and 108 are top plan and cross-sectional views, respectively, of another embodiment of a waveguide coupler with a waveguide mirror according to the present inventions.

5 FIGS. 109-111 show schematic side views of additional three-dimensional OE stack configurations according to the present inventions.

FIG. 112 shows schematic side views of additional exemplary stacking configurations of OE films using Z-connections according to the present inventions.

FIGS. 113-116 show schematic side views of various exemplary OE films according to the present inventions.

10 FIGS. 117-120 show schematic side views of exemplary film optical link modules (FOLM) embodiments according to the present invention.

FIG. 121 shows a schematic top view of an OE film of an FOLM structure according to the present inventions.

15 FIGS. 122 and 123 are schematic top and side views, respectively of an further embodiment of a FOLM OE film according to the present inventions.

FIGS. 124 is schematic perspective view of an further embodiment of a FOLM OE film according to the present inventions.

FIG. 125 is a schematic side view of another FOLM embodiment according to the present invention.

20 FIG. 126 shows a schematic side view of a exemplary Film Optical Link Module (FOLM) embodiment according to the present invention.

FIG. 127 shows a top plan view of the embodiment shown in FIGS. 126.

FIG. 128 shows a schematic side view of a portion of the FOLM embodiment of FIG. 126 according to the present invention.

25 FIG. 129 shows a top plan view of the polymer layer in the embodiment of FIG. 128 which has an opto-electronic device embedded therein according to the present invention.

FIG. 130 shows an opto-electronic interposer (OE-IP) embodiment suitable for chips, chip size packages (CSPs), and multichip modules (MCMs) according to the

present inventions.

FIG. 131 shows another OE-IP embodiment suitable for multichip modules (MCMs) according to the present inventions.

FIGS. 132-134 show additional OE-IP embodiments suitable for multichip  
5 modules (MCMs) according to the present inventions.

FIG. 135 shows an another OE-IP embodiment with optical interconnections to chips/MCMs mounted to both sides of the OE-IPs according to the present inventions.

FIGS. 136-137 show OE-IP embodiments with external and flexible interconnections according to the present inventions.

FIG. 138 shows an OE-IP embodiment where the optical interconnections of the interposer are on the opposite side of the chip/CSP/MCM according to the present  
10 inventions.

FIG. 139 shown an embodiment having an OE-IP film and MCM according to the present inventions.

FIG. 140 shown an OE-film-MCM embodiment according to the present  
15 inventions.

FIGS. 141-142 show smart pixel embodiments according to the present inventions.

FIG. 143 shows an opto-electric (OE) printed circuit board/mother board  
20 embodiment according to the present inventions.

FIGS. 144-146 show respective OE film embodiments useful for both intra-MCM and inter-MCM optical connections according to the present invention.

FIGS. 147-153 show schematic side views of an exemplary structure being fabricated by an exemplary process to fabricate an OE film with embedded devices  
25 according to the present inventions.

## **DETAILED DESCRIPTION OF THE PRESENT INVENTION**

FIG. 1 shows an expanded perspective view of a first embodiment of an opto-electronic (optical-electronic) interconnect substrate according to the present

invention at reference number 10. The interconnect substrate 10 takes the form of an opto-electronic multichip module (OE-MCM) substrate that interconnects signal from one or a plurality of I.C. chips 1a-1d, including both inter-chip and intra-chip connections, by both optical links and electrical traces. Substrate 10 comprises a base substrate 12 and an active layer 20. The active layer comprises optical waveguides 24a-24h, opto-electronic switching devices 26a-26c, photo-detector devices 28a-28c, electrical traces 30, and electrical connection pads 32 for the I.C. chips 1. The I.C. chips are flip-chip assembled to active layer 20 and are electrically coupled to the connection pads 32 of layer 20 by a plurality of any type of conventional connectors 2. For the example, as shown in FIG. 1, connectors 2 may comprise solder bumps. The optical waveguides 24 and the opto-electronic devices 26 and 28 are incorporated into active layer 20, and are preferably embedded therein such that the top surface of layer 20 is substantially flat (*e.g.*, having a surface uniformity that is within  $\pm 10\ \mu\text{m}$  over a 1 cm square area, except for small holes, grooves, bumps, *etc.*).

Signals between the chips may be conveyed electrically by traces 30 or optically by waveguides 24. When the signals are conveyed by light (*i.e.*, optically) on waveguides 24, the opto-electronic devices 26 and 28 provide the conversions between light and electrical representations of the signals. As one example of how light may be used to convey a signal, a light power source is brought to OE-MCM substrate 10 by optical fiber 4 and is coupled to optical waveguide 24a. (A light power source may provide a continuous source of light energy during the operation of the circuit or system formed by chips 1, or it may provide a pulse train of light pulses.) The coupling between fiber 4 and waveguide 24a may be accomplished by a standard V-groove connector 14, whose construction is well known to the optical-fiber communication art. It is also possible to connect optical fibers to the waveguides at the layer's surface by incorporating  $45^\circ$  mirrors, gratings, *etc.*, within the core material of the layer and by positioning each fiber so that its core is aligned to a mirror or grating. The light source propagates along waveguide 24a and is divided among two waveguides 24b and 24c by a conventional Y-branch divider in a pre-selected ratio (such as 50%-50% if the light is not

divided in further stages, or if the light in each branch is divided again in further stages, or such as 33%-67% if the light in one branch is divided again in a further stage). The light in waveguide 24b is routed to an opto-electronic switch 26a, which selectively routes the light onto waveguide 24d depending upon the electrical signal provided to the switch. The electrical signal is provided to switch 26a by two connection pads 32, which in turn are coupled to circuitry on chip 1a through solder-bump connectors 2. In this manner, an electrical output signal from circuitry on chip 1a is converted to an optical representation on waveguide 24d by switch 26a.

From switch 26a, waveguide 24d is routed to a second electrical-optical switch 26b, which has an electrical input which is coupled to circuitry in chip 1d by similar pads 32 and connectors 2. Switch 26b has one optical input, which is coupled to waveguide 24d, and one electrical input, which is coupled to circuitry on chip 1d. Switch 26b also has two optical outputs, which are coupled to waveguides 24e and 24f, respectively. Depending upon the electrical input to switch 26b, switch 26b will either route the light at its optical input to one of its optical outputs or the other. An exemplary construction for switch 26b is described below with reference to FIGS. 2 and 3. The optical signals on waveguides 24e and 24f are provided to two photo-detector devices 28b and 28c, respectively. Photo-detector devices 28b and 28c convert their respective light signals to corresponding electrical representations, and provide their representations to input circuits on I.C. chips 1c and 1d, respectively, through corresponding connection pads 32 and connectors 2. Switch 26b is not always used or necessary in this situation. In such a case, the substrate does not contain the routing switch and the output of waveguide 24d may be directly connected to receiver 28b or 28c, or to both receivers.

In a similar manner, the light power source on waveguide 24c is routed to an opto-electronic switch 26c, which is controlled by an electrical output signal from I.C. chip 1b. From the optical output of switch 26c, the modulated light output is routed onto waveguide 24h, which terminates in an optical fiber 5, to be transported off of OE-MCM substrate 10. A conventional V-groove connector 15 is used to coupled fiber 5 to waveguide 24h. As indicated above, it is also possible to connect optical fibers to the

waveguides at the layer's surface by incorporating 45° mirrors, gratings, etc., within the core area (where the waveguide mode propagates) of the layer and by positioning each fiber so that its core is aligned to a mirror or grating. Referring back to waveguide 24c, which provides the input to switch 26c, it will be noticed that it crosses at a near right angle with waveguide 24d. The crossing is a conventional optical waveguide intersection, and results in a minimal amount of light crossing over from waveguide 24c to waveguide 24d, and *vice versa*.

Photo-detector devices may also be used to receive optical signals from outside of OE-MCM substrate 10. An example is shown with photo-detector 28a, which receives a light signal from an optical fiber 3 through waveguide 24g. A conventional V-groove connector 13 is used to couple fiber 3 to waveguide 24g. As indicated above, a 45° mirror, grating, etc., may also be used. The electrical output of photo-detector device 28a is provided to input circuitry on I.C. chip 1c through connection pads 32 and connectors 2.

Although it is not shown in the figure, the optical waveguides can be routed from one terminal of a chip to another terminal of the same chip, thereby providing intra-chip optical interconnection.

The number of waveguides 24, devices 26 and 28, electrical traces 30, interconnection pads 32, fibers 3-5, and chips 1 shown in FIG. 1 have been kept to a low number for the sake of visual simplicity. With the possible exception of chips and fibers, a typical OE-MCM substrate 10 has many more of these components than shown. Also, the size of the components has been exaggerated for the sake of visual clarity. Typical widths of waveguides 24 can be on the order of 1 μm to 50 μm, and typical dimensions of I.C. chips are 1 cm to 4 cm on a side. Typical widths of devices 26 and 28 can be on the order of 1 μm to 50 μm (the width is the shorter of the two horizontal surface dimensions). Typical lengths of devices 26 and 28 can be on the order of 1 μm to 5,000 μm (the length is the longer of the two horizontal surface dimensions). Typical thicknesses (the vertical dimension) of devices 26 and 28 are less than 30 μm, and can be in the range of 1 μm to 20 μm. Typically, the larger sized devices are used in free-space

optical connection applications. Although FIG. 1 shows that each device 26 and 28 is provided with two electrical connections from a corresponding I.C. chip, it may be appreciated that active layer 20 may comprises a ground plane (or power plane) within it, and that a device 26 or 28 may have one of its electrical terminals connected to this plane and its other electrical terminal coupled to an output or an input of a corresponding I.C. Instead of fibers 3-5, array fibers, film waveguides, or imaging guides can be used.

FIG. 2 shows a partial cross-sectional view of active layer 20 in the vicinity of opto-electronic switch 26c, and FIG. 3 shows a top plan view of switch 26c in relation to waveguides 24c and 24h. Referring to FIG. 2, active layer 20 comprises a patterned layer 24 of core material approximately 5  $\mu\text{m}$  thick, from which the individual waveguides 24a - 24g are formed, such as waveguides 24c and 24h. The waveguide layer is formed above an optional cladding layer 21 (if base substrate 12 is not suitable as a cladding layer), and is covered over by a second cladding layer 23. Cladding layer 23 extends over the sides of waveguides 24 as well as the tops of waveguides. As is known in the art, optical waveguides can be made from two types of materials having two different indices of refraction ( $n_1$  and  $n_2$ ), which are called the core material and the cladding material. The core material has the higher index of refraction. Cladding layers 21 and 23 may have different indices of refraction, as long as they are both less than the index of refraction of core layer 24. The cladding layer may comprise, for example, Hitachi's fluorinated polyimide OPI-N1005 (Hitachi Chemical Co.) and the core layer may comprise, for example, Hitachi's fluorinated polyimide OPI-N3405 (Hitachi Chemical Co.). If base layer can function as a suitable cladding layer, then cladding layer 21 may be omitted.

Switch 26c is embedded in active layer 20, with its bottom surface against the top surface of base substrate 12. There are a number of different types of opto-electronic switch devices that can be used. Such examples are an internal total-reflection switch, a Mach-Zehnder modular, a digital switch, grating-type switch, electro-absorption (EA) light modulator, semiconductor optical gate switch, *etc.* The exemplary switch device shown in FIG. 2 is an internal total-reflection switch, and it comprises a body of electro-optical (EO) material 626 which changes its refractive index when an electric field is



applied across it. Referring to FIG. 3, the body of EO material 626 is formed in a Y-shaped body having a through section between waveguide 24c and a second output waveguide 24i, and a branch section from this through section to output waveguide 24h. Material 626 is placed in the path between input waveguide 24c and output waveguides 24h and 24i, and is positioned between cladding layers 21 and 23. The field is applied by two opposing electrodes 27, which also serve as the electrical terminals of the device. Short electrical traces, which are not present in the cross-sectional plane of FIG. 2, connect electrodes 27 to respective connection pads 32, which are not present in the cross-sectional plane of FIG. 2 but whose locations in back of the plane are shown by dashed lines. When no potential is applied across electrodes 27, light travels along the through section from waveguide 24c to waveguide 24i. When an electrical potential difference is applied between electrodes 27, a portion of the EO material 626 undergoes a change in its index of refraction, which in turn changes the propagation direction of the light so a major portion of the light goes into the output waveguide 24h. More specifically, the light encounters a lower index of refraction at the section of EO material 626 located between electrodes 27, and is reflected to the branch section. EO material 626 may comprise organic materials, including electro-optic polymers, such as those disclosed in U.S. patent No. 5,444,811, assigned to the assignee of the present application and incorporated herein by reference. EO material 626 may also comprise multiple quantum well devices and quantum dots made from exemplary III-V compounds, such as  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  /  $\text{Al}_y\text{Ga}_{1-y}\text{As}$ . When applying a reverse voltage bias, these devices are able to change their indices of refraction as a function of the applied bias.

In general, active layer 20 is formed by a built up technology. As used in this application, a build-up technology refers to any combination of film layer deposition steps, waveguide patterning steps, embedding of EO devices, and formation of vias and contact layers to form a film with embedded waveguides and/or embedded EO devices. As one example, cladding layer 21 is first formed over base substrate 12, followed by the formation and patterning of optical core layer 24, followed by the formation of cladding

layer 23, and then followed by the formation of electrical traces 30 and interconnect pads 32. The opto-electronic devices 26 and 28 may be formed individually and then incorporated into active layer 20 after or while cladding layer 21 is formed, and before core layer 24 is formed. In some cases, the devices can be formed while the layers 21-24 are being formed. For example, the bottom electrode of switch 26c (see FIG. 2) may be formed before cladding layer 21 is formed. After cladding layer 21 is formed, a square of EO material is formed where switch 26c is to be located. Thereafter, the surface may be over-coated with core material for layer 24 and cured. The surface is then planarized to expose the top of the square of EO material 626. Both the core layer and the square of EO material 626 are then patterned (such as by conventional patterning of a photoresist layer, or a mask layer, followed by etching) to form the pattern of the waveguides 24c and 24h and the final Y-branch shape of EO material 626. Cladding layer 23 and a metal layer for top electrode 27 and pads 32 are then formed.

#### **DESCRIPTION of FIGS 4-1, 5-1, 4-2, 5-2, 4-3, and 5-3.**

FIG. 4-1 shows a partial cross-sectional view of active layer 20 in the vicinity of photo-detector device 28c, and FIG. 5-1 shows a top plan view of device 28c in relation to waveguide 24f. Like switch 26c, photo-detector device 28c is embedded in active layer 20, with its bottom surface against the top surface of base substrate 12. There are a number of different types of photo-detector devices that can be used. The exemplary detector device shown in FIGS. 4-1 and 5-1 comprises a body 628, or mini-chip, of semiconductor material and two electrodes 27 formed at the top surface of body. For visual simplicity, two simple straight electrodes are shown in the figures. Typical MSM photo-detector devices used by the present application have interdigitated electrodes for increasing hole-electron collection efficiency. The exemplary device 28c is independently constructed and then placed on top of cladding layer 21 and adhered thereto prior to forming waveguides 24a-24i. The material of body 628 is capable of generating a voltage across its electrodes 27, and/or a current across its electrodes 27, and/or a change in conductivity across its electrodes 27. For example, body 628 may

comprise a semiconductor material with a p-n junction formed in the material, with the p-type doped region electrically coupled to one electrode 27 and the n-type doped region electrically coupled to the other electrode 27. The p-n junction generates a current when exposed to light, and this current may be detected by conventional detection circuitry known to the photo-detection art. As another example, body 228 may comprise a semiconductor material that has a p-i-n junction or an n-i-p junction formed in the material, with the doped regions electrically coupled to respective electrodes 27. When the intrinsic (i) semiconductor region is exposed to light, the concentration of electrons and holes is increased, and the conductivity of the region is increased. This changes the conductivity between electrodes 27, which can be detected by conventional detection circuitry known to the photo-detection art. Also, a simple body of intrinsic (i) semiconductor, with two ohmic contacts to it, may be used. More complex devices, such as bipolar photo-transistors and field-effect photo-transistors, may be used. The construction of these devices are well known to the art, and can be adapted in view of the present application to position the photon-collection areas to one or more sides of the mini-chip of semiconductor material. In FIG. 4-1, the thickness of the photodetector layer is shown as being almost the same as that of the core layer thickness of the waveguide. However, more generally it is preferably to make the thickness of the photodetector larger than that of the core layer thickness in order to achieve efficient light absorption in the photodetector.

As previously indicated, the exemplary device 28c is independently constructed and then placed on top of cladding layer 21 and adhered thereto prior to forming waveguides 24a-24i. In the case that cladding layer 21 comprises a polymeric material that is initially dispensed in liquid form and then cured, device 28c may be set into layer 21 while layer 21 is in a liquid or tacky state, and then may be firmly adhered to layer 21 during the curing process. If cladding layer 21 comprises a laminated layer, or otherwise cured or non-adhesive layer, a body of polymeric adhesive may be applied to the back of device 28c before placement, and then cured to adhere device 28c to layer 21. After being set in place, the waveguides 24a-24i and top cladding layer 23 are formed in

sequence, with vias being formed to electrodes 27 of device 28c. A top metalization layer is formed for providing traces 30 and pads 32, as shown in solid lines in FIG. 5-1.

The device of FIG. 4-1 can have fingered electrodes, such as those found in interdigitated electrodes. One of the fingered electrodes may be formed on the bottom surface of the device's chip. In this case, a contact to the bottom electrode is made by diffusion bonding a portion of the electrode to a electrical trace formed on the surface of the base substrate (or formed on a cured layer 21). AuSn bonding, AuSnIn bonding, AuIn bonding, and Pd bonding can also be used. High temperature underfill material is then preferably dispensed to fill the air pockets underneath the component that has been diffusion bonded. Cure material can also be used to fill the air pockets.

The photodetectors used in the present application are not restricted to being interdigitated types. For example, a sandwich-type electrode configuration is possible. Also, the detector's bottom surface (the surface in which light enters the detector) may have an electrode with a window to receive light, and may have a second electrode located at the detector's top surface.

FIGS. 4-2, 5-2, 4-3, and 5-3 show two additional preferred photo-detector embodiments at reference numbers 28c' and 28c'', respectively. Although these examples are for vertical-type photodetectors, the arrangements and considerations apply to lateral-type photodetectors as well. As is well-known, a load resistor is required to output voltage signals from a photo-detector. As shown in FIGS. 4-2 and 5-2, a load resistor 29 is integrated into the ELO photodetector 628. Alternately, a preamplifier may be integrated into the ELO detector 628, such as at the location of resistor 29. FIGS. 4-3 and 5-3 show an alternate load resistor 29' comprised of a serpentine NiCr film with, for example, a thickness of 300nm, a width of 3 microns, and a total length of 500 microns.

While photo-detectors are one example where an appropriate impedance matching electrical circuit such as an amplifier or load resistor is required for proper device operation, more generally an appropriate resistor, capacitor, driver, or other circuit may be required to couple other electrical or opto-electronic devices, such as a laser diode, to the power supply (or to ground or other electrical and/or opto-electronic devices). In the

illustrations of the present invention shown in the figures, only two electrodes per device are shown. However, more generally, each device may have a plurality of power and/or signal electrodes in a similar manner to non-embedded devices.

FIG. 6 shows an expanded perspective view of a second embodiment of an opto-electronic interconnect substrate according to the present invention at reference number 10'. The interconnect substrate 10' is similar to substrate 10 shown in FIG. 1, and takes the form of an opto-electronic multichip module (OE-MCM) substrate that interconnects signal from one or a plurality of I.C. chips 1a-1d by both optical links and electrical traces. Common reference numbers have been used to designate common elements of substrates 10' and 10. As one difference, substrate 10' uses light emitting devices 36a and 36b in place of the opto-electronic switch devices 26a and 26b of substrate 10. The light emitting devices 36 do not need an outside source of light, such as provided by optical fiber 4 of substrate 10, and thus substrate 10' does not require optical fiber 4. Device 36 may comprise a light-emitting diode (LED), a laser diode (LD), a vertical cavity surface emitting laser (VCSEL), quantum-well or quantum-dot devices (under forward bias), or other light-emitting devices.

FIG. 7 shows a partial cross-sectional view of an exemplary light-emitter device 36b, and FIG. 8 shows a top plan view of device 36b in relation to waveguide 24h. Like switch 26c, light-emitter device 28c is embedded in active layer 20, with its bottom surface against the top surface of base substrate 12. Light emitter device 36c comprises a body 636, or mini-chip, of light-emitting material, such as semiconductor, and two electrodes 27 formed at the top and bottom surfaces of body 636. Device 36b emits light from one or more of its sides, and may comprise a light-emitting diode or laser diode formed in semiconductor material. The exemplary device 36b is independently constructed and then placed on top of an electrode disposed on or in cladding layer 21 and adhered thereto prior to forming waveguides 24a-24i, such as by the adhesion steps described above, including solder or metal-diffusion processes. The construction of these devices are well known to the art, and can be adapted in view of the present application to position the photon-emission areas to one side of the mini-chip of semiconductor

material.

During construction, the placement of device 36b on cladding layer 21 and the patterning of waveguide 24h are performed with the use of alignment marks on base substrate 12. During fabrication, there may be some misalignment of device 36b or the pattern for optical waveguide 24h with respect to these marks, and consequently there may be some misalignment between the optical output of device 36b and the optical input of waveguide 24h. To account for any such misalignment, the optical input of waveguide 24h may be flared, or tapered outward, as shown in FIG. 8. If there is mis-alignment, the taper ensures that the light from device 36b directed into the optical waveguide.

This potential for misalignment is also of concern for making the via contacts from traces 30 to electrodes 27. This may be addressed by designing additional tolerances into the via dimensions (*e.g.*, using larger dimensions than the minimum dimensions imposed by the lithography and etching steps employed). One may also elongate the shapes of traces 30 and electrodes 27 in the via area, and arrange the elongated shapes to intersect at 90° angle.

FIG. 9 shows a partial cross-sectional view of a second exemplary light-emitter device 36b', and FIG. 10 shows a top plan view of device 36b' in relation to waveguide 24h. Device 36b' comprises a vertical cavity surface emitting laser (VCSEL) 638 formed on a semiconductor mini-chip (or die) 636. The VCSEL element 638 generates light which is directed perpendicular to the top surface of mini-chip 636, which is different from the previous example where the light was generated at a side of the mini-chip. Substrate 636 lies below core layer 24, and a mirror 639 is positioned in front of VCSEL element 638 to reflect the vertical light beam of element 638 into waveguide 24h, and thereby along a horizontal direction. The surface of mirror 639 is preferably at a 45° angle to the element's light beam. One end of optical waveguide 24h is located over VCSEL element 638 and is beveled at an angle (preferably at a 45° angle) with respect to the normal vector of the substrate surface. (The normal vector is the vector which is perpendicular to the top surface of base substrate 12). The beveling may be accomplished by laser abrasion using a laser that is tilted at a 45° angle with respect to the normal

vector of the substrate surface. Reactive ion etching (RIE) methods may also be used. If photosensitive materials are used, tilted lithographic exposures may be used. Mirror 639 is built upon the beveled surface, such as by depositing a reflective metal or reflective material over this area. Exemplary reflective metals include silver (Ag), aluminum (Al), gold (Au), copper (Cu), chromium (Cr), tungsten (W), titanium (Ti), etc., and exemplary reflective materials include multilayer dielectric coatings comprising such materials as titanium dioxide ( $\text{TiO}_2$ ), silicon dioxide ( $\text{SiO}_2$ ), alumina (aluminum oxide  $\text{Al}_2\text{O}_3$ ), zinc oxide ( $\text{ZnO}$ ), chromium oxide ( $\text{Cr}_2\text{O}_3$ ). The angle of mirror 639 may vary from a value of  $45^\circ$  by small amounts, depending upon the difference in the index of refraction of the core and cladding layers. If the difference in the indices of refraction is  $\Delta n=0.02$ , then a maximum angle deviation of  $\pm 3^\circ$  can be tolerated. Given the value of  $\Delta n$ , it is well within the skill of the art to compute the maximum angle deviation. As used herein, a  $45^\circ$  angle or an angle of approximately  $45^\circ$  compasses all angles within the angle tolerance for the corresponding value of  $\Delta n$ ; thus angles from  $42^\circ$  to  $48^\circ$  are encompassed for a  $\Delta n$  of 0.02, which has the above angle tolerance of  $\pm 3^\circ$ . Instead of mirror 639, an optical grating may be used. An optical grating may comprise a sequence of material layers having alternating indices of refraction  $n_1$  and  $n_2$  and being formed at a  $45^\circ$  angle to the substrate normal vector. Such an optical grating may be constructed by forming a set of spaced cuts in the end of waveguide 24h, and then filling the cuts with an optical material having a different index of refraction. The set of  $45^\circ$  angle cuts is most readily obtained by using a photosensitive optical material and passing the exposure radiation through a optical device which generates an interference pattern which has closely spaced, alternating regions of high and low intensity light. The interference pattern is tilted at an approximate  $45^\circ$  angle to the normal vector of the substrate and focused on the region where the grating is to be formed. As in the mirror case, small angle deviations can be tolerated, and the tolerance can be computed from the indices of refraction by those of ordinary skill in the optics art. The gratings may also be formed by anisotropic etching methods which are described in greater detail below with reference to the devices illustrated in FIGS. 22-25.

As shown in FIG. 9, device 36b' is embedded in a material layer 25b, which underlies cladding layer 21. To ensure that device 36b' is attached to base substrate 12, an adhesive layer 25a may be formed over base substrate 12 prior to forming material layer 25b. Layers 25a and 25b may comprises any suitable polymeric material, include the material of cladding layer 21 or core layer 24, as well as conventional polyimide materials. The preferably comprises the same material, but the can be different. The electrodes 27 of device 36b', as well as other component devices, may be located on the bottom surface of the device, or on both surfaces (so called opposing electrodes). In this case, the bottom electrodes can be diffusion bonded to electrical traces formed on the surface of the base substrate (or formed on a cured layer 25a). High temperature underfill material is then preferably dispensed to fill the air pockets underneath the component that has been diffusion bonded. Also, the material of layer 25b can fill the air gap. When a VCSEL is used, a vertical-type photodetector may be embedded using a similar process and having a configuration similar to that shown in FIGS. 9-10.

#### **Exemplary Construction Methods, FIGS. 11-20.**

Exemplary methods for constructing active substrate 20 for substrates 10 and 10' are described with respect to FIGS. 11 - 18, which show cross-sections of the layers of active substrate 20 during construction. In the cross-sections shown, a opto-electronic switch device 26 and a photo-detector device 28 will be formed adjacent to one another with an optical waveguide being routed from an optical output of device 26 to an optical input of device 28, as finally shown in FIG. 18.

Referring to FIG. 11, a bottom electrode 27 of switch device 26 is formed on the top surface of base substrate 12 by conventional deposition and photo-lithographic steps that are well known to the art. In addition to forming electrode 27, alignment marks for further processing steps may be formed, or these alignment marks may be etched in the surface of base substrate 12 prior to forming electrode 27. As the next step, cladding layer 21 is formed, such as by spin-coating a fluidized polymer over base substrate 12. In order to attach components 28, a material for layer 21 is selected



which has adhesive capabilities, such as Hitachi's fluorinated polyimide OPI-N1005 or a solvent-free (non-gaseous) epoxy materials. The thickness of layer 21 may range between 1  $\mu\text{m}$  and 20  $\mu\text{m}$ , after any shrinkage from a subsequent curing step.

Individual optical-electric components, such as device 28, are placed on top of layer 21 and adhered thereto, preferably before the fluidizing solvent of layer 21 is completely evaporated away from layer 21. Non-solvent based materials may also be used for layer 21, such as epoxy materials. (In general, epoxy materials decompose at a lower temperature than polyimide materials, which should be taken into account when choosing the material for subsequent layers). Layer 21 is then soft-baked to remove the fluidizing solvent (if it present) and to perform some optional partial cross-linking of the polymeric material. Layer 21 is then cured by steps that are appropriate for its material composition, such as by exposure to heat, radiation, time, or a combination thereof. The evaporation of the solvent is performed gradually to accommodate the lateral diffusion of the solvent which underlies the individual components (28). With some cladding materials, one can perform a partial soft-bake step to make the surface of layer 21 tacky before the individual components are placed. The partial soft-bake reduced the time required to laterally diffuse out the fluidizing solvent that is under the set components (e.g., 28).

The back side of each placed component (e.g., 28) may be coated with chromium prior to the adhesion step in order to improve adhesion of the components to the polymeric material of layer 21. In some cases, the chromium film may be patterned to form bottom electrodes of the component. Commercially available surface mounting equipment, flip-chip bonding equipment, or a custom purpose aligner may be used to position the components. Alignment marks may be included on the individual components (e.g., 28) and/or base substrate 12 for this purpose. Instead of making alignment marks on individual components, it is also possible to make marks on several components or on several points of the substrate portion on which the components are disposed. Surface mount equipment, flip chip equipment or a custom purpose aligner

can place components to within  $\pm 2 \mu\text{m}$  to  $\pm 5 \mu\text{m}$ .

As indicated above, the thickness of the individual components (*e.g.*, 28) is preferably relatively thin, such as on the order of  $1 \mu\text{m}$  to  $20 \mu\text{m}$ . Such thin O/E components can be manufactured using the vapor phase epitaxial liftoff process described by Yablonovitch, "Vapor Phase Epitaxial Liftoff Process of GaAs", the Fall 1997 Materials Research Symposium. Other processes, such as liquid phase epitaxial liftoff or polishing may also be used as well. The epitaxial lift-off (ELO) process takes advantage of the very large difference in etch rate between GaAs (Gallium Arsenide) and AlAs (Aluminum Arsenide), or between GaAs and  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  (Aluminum Gallium Arsenide) with large  $x$ , in hydrofluoric acid. Starting with a GaAs substrate, a layer of AlAs is formed over the top surface by epitaxial growth (*e.g.*, MBE, OMVPE, *etc.*). Layers of GaAs and  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  are then formed over the AlAs layer, also by epitaxial growth. Opto-electronic devices are then formed in the top GaAs layer, including electrodes and a top passivation layer. (For the present invention, a polish-stop layer is formed on top of the passivation layer and electrodes, as described below). Deep trenches are then formed in the top GaAs layer to separate the devices into individual components or individual array chips (which are chips containing multiple devices). (Such array chips are usefully in implementing optical buses where multiple signals are grouped together and routed from a bank of optical switch devices (or emitters) to a bank of photo-detectors.) As a supporting substrate, a polymer film, such as Mylar, or glass, quartz, is then laminated to the top surface of the GaAs components, including the array chips. The entire substrate is then exposed to a hydrofluoric acid etch, which etches the AlAs layer laterally and results in the release of the GaAs and  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  components (*e.g.*, mini-chips) from the GaAs substrate while still being attached to the polymer film (when a polymer is used for the supporting substrate). The components may then be cut from the polymer film, or they may be held by the film until used. In the latter case, layer 21 is soft-baked to a point where it has more tacky adhesion force than the laminated polymer film; when the component is pressed in the tacky layer 21, it is retained on layer 21 when the laminated polymer film is pulled away, and it

separates from the polymer film. As another option, one may deposit metal on the exposed bottom surfaces of the epitaxial devices while they are still attached to the carrier film. Corresponding metal pads may be formed on a cured layer 21, and the epitaxial devices may then be attached to the corresponding metal pads by diffusion bonding, AuSn bonding, AuInSn bonding, AuIn bonding, Pd bonding, or other similar bonding processes. Dimensional stability is improved if rigid substrates, like glass, are used for the supporting substrate.

It is believed by the authors that a similar epitaxial lift-off process may be developed for a silicon (Si) substrate using an intermediate SiGe (Silicon Germanium) layer in place of the AlAs layer, and by using an etchant which differentiates between SiGe and silicon (Si). This would enable a high-yield ELO process to be performed for silicon chips.

In subsequent processing steps, a layer of core material will be formed over the individual components (*e.g.*, 28), and the resulting surface will be exposed to a polishing step to make the surface more planar. In preferred construction implementations, the polishing step will remove parts of the core material which overlay the electrodes 27 of the individual components (*e.g.*, 28) and expose the top surfaces of the electrodes 27. For this purpose, the electrodes 27 preferably have an initial height which is greater than normally required, and they are then ground down by the polishing step. In addition, the electrodes 27 preferably have a composite structure of two or more metal sub-layers, with one of the sub-layers comprising a polish-stop material, such as tungsten. An example is shown in FIG. 11, where electrodes 27 comprise a bottom sub-layer 27x of copper, a middle sub-layer 27y of tungsten, and a top sub-layer 27z of copper. The tungsten sub-layer 27y may have a thickness in the range of 0.1  $\mu\text{m}$  to 1  $\mu\text{m}$ , and copper layer 27x and 27z may have thicknesses of 2  $\mu\text{m}$  to 20  $\mu\text{m}$ . To reduce copper diffusion during polymer curing, the top surface of the copper can be capped by a diffusion barrier layer (*e.g.*, titanium or nickel layer). Other metals, such as Au, may be used instead of Cu. In a slurry having alumina particles as the abrasive, copper polishes at a faster rate than tungsten.

After layer 21 is cured, or between the time layer 21 is soft-baked and cured, layer 21 may be patterned to form vias to bottom electrode 27. This is most easily accomplished by laser drilling the via apertures and then filling the apertures with conductive materials, such as for example copper. The location of the via is indicated in FIG. 11 by the term "via". In place of laser drilling, the via apertures may be formed by etching through a thick photoresist layer which has been photolithographically patterned with apertures which correspond to those to be formed in layer 21. If layer 21 has been cured, then dry etching is preferred; wet etching is usually best used with a soft-baked and uncured layer 21. As indicated below, the via in layer 21 may also be formed at a later step.

The via apertures in layer 21 may be filled with conductive material by a number of conventional deposition methods, including sputtering conductive material (*e.g.*, copper), chemical vapor deposition (CVD), and plating conductive material. Electroless plating, direct plating (electroplating), and CVD may be used to fill the via apertures without depositing material over the entire substrate. Electroless plating is, however, relatively slow. Other methods deposit conductive material over the entire surface and then etch away the material in those areas where it is not wanted. Before performing such a blanket deposition of material, it is advisable to cover the placed components (*e.g.*, 28) with a protective patch of photoresist material so that the subsequent etching operation does not harm these components, particularly their metal electrodes. If electro-plating is used, a conductive seed layer is first sputtered over layer 21 to provide a conductive path for the plating current. The seed layer usually comprises a thin chromium adhesion layer (*e.g.*, 200 Å) followed by a thicker copper layer (*e.g.*, 2 μm). The excess conductive material is removed by conventional chemical etching using masking caps over the filled via apertures. The masking caps can be easily formed by coating a layer of photoresist over the newly deposited copper layer, and thereafter pattern exposing and developing the photoresist layer. After the excess copper (and any seed layer) is etched away, the masking caps are removed by a suitable stripper or solvent. The above described via formation steps may be used to

form vias in other dielectric and polymeric layers described herein.

Referring to FIG. 12, a layer EO material 626 for switch device 26 is formed over layer 21 and the individual components (e.g., 28). The layer of EO material 626 is then patterned to leave a portion (or body) of the material in the location where switch device 26 is being formed. The portion left is typically a course portion of the material and is not in the final pattern of the body of EO material 626 which will be used for device 26. For example, it may be a generally rectangular portion (as viewed from the top surface of base substrate 12) which encompasses the body of EO material 626 that will actually be used for switch 26 (see FIG. 19). A subsequent step will typically do the final patterning of this portion of EO material 626 (see FIG. 20). This course patterning of the layer of EO material 626 may be done by any number of conventional patterning techniques. If EO material 626 is photo-imageable, it may be patterned exposed to actinic radiation and thereafter developed. If it is not, a photoresist layer may be formed over the layer of EO material 626, and the photoresist may be patterned to leave an etch mask which covers the course portion of EO material 626 which is to be retained. Both wet and dry etching steps may be used to remove the unwanted portions, with dry etching being preferred as these etching processes are anisotropic and provide sharper vertical walls. Plasma dry etching techniques may be used, and the photoresist layer may be sacrificed during the dry etching process as long as a portion of its thickness remains by the end of the etching process.

In FIG. 12, a further embodiment of these possible patterning methods is preferably used. Specifically, a tungsten layer having a thickness of  $0.1\ \mu\text{m}$  to  $1\ \mu\text{m}$  is formed over the layer of EO material 626, and this tungsten layer is patterned to leave tungsten etch masks 627 for portions of EO material 626 that are to be retained. The patterning may be done by forming a photoresist layer over tungsten layer 627, patterning and developing the photoresist to expose the unwanted tungsten, and then etching the unwanted tungsten, such as by a hydrogen peroxide solution. FIG. 13 shows the result of the pattern etching of the layer of EO material 626. The tungsten etch mask 627 will be used in a subsequent polishing step as a polish-stop layer for

protecting the retained portions of EO material 626, and thus it will serve two purposes. It may be appreciated that other materials may be used in place of tungsten, and that the construction methods of the present invention are not limited to using tungsten. For example, other metals, deposited silicon dioxide, and deposited silicon nitride may be used. The etch mask can, if necessary, be used as a poling electrode to enhance the electro-optic coefficient of the EO material.

Instead of forming the portions of EO material 626 by spin-coating, CVD, or MLD, one can place chips of semiconductor material which have electrical-optic properties or electro-absorption properties. For example, multiple quantum-well devices comprising alternating layers AlGaAs and GaAs (or InGaAlAs (Indium-Gallium-Aluminum-Arsenide) or InGaAsP (Indium-Gallium-Arsenide-Phosphorus), *etc.*), change their index of refraction (or electro-absorption properties) as a function of applied potential difference. These chips may be made by the epitaxial liftoff process described above, and they may be placed down onto layer 21 at the same time that components 28 are placed down onto layer 21 (either with simultaneous placement or sequential placement). This possibility is shown by the dashed chip of material 626' in FIG. 11. In this case, the step of coating the layer of polymeric EO material 626 exemplified by FIG. 12 may be omitted, as well as the steps of defining and curing the coated material 626 (unless of course one wants to use both materials 626 and 626' in the same active substrate 10). A polish-stop layer 627 is preferably formed over the chip 626', preferably before placement. Layer 627 may then be patterned to define the final shape of chip 626', and the semiconductor chip can then be etched to remove those portions of semiconductor which are not underneath the patterned layer 627, before the core layer is formed. The processing of chip 626' is thereafter the same for those steps exemplified in FIGS. 13-20.

Referring to FIG. 14, the next step is to form a layer 24 of optical core material over cladding layer 21, the individual components (e.g., 28), and the portions of EO (or EA) material 626. For this purpose, a spin coat step may be used, where the core material comprises a polymer material which has been fluidized (*i.e.*, made into a

viscous fluid) with a solvent. In this regard, and as mentioned above, the fluidized core material may comprise, for example, Hitachi's fluorinated polyimide OPI-N3405 (Hitachi Chemical Co.). Layer 24 is then exposed to a softbaking step to remove the fluidizing solvent, and then to a curing step which is appropriate for its material composition, such as by exposure to heat, radiation, time, or a combination thereof. Guidelines for the softbaking and curing of core materials, cladding materials, and electro-optical materials are provided by the manufacturers. The thickness of layer 24 is preferably greater than 90% of the thickness of the component mini-chips (e.g., 628) or the thickness of the portions of EO material 626, whichever is less, and is more preferably thicker than the mini-chips and the portions of EO material 626. Typical thicknesses of the initially-formed and cured layer 24 are less than 30  $\mu\text{m}$ , and more typically in the range of 3  $\mu\text{m}$  to 20  $\mu\text{m}$ .

Referring to FIG. 15, the surface of the substrate is polished to make it more planar. The polishing step removes the portions of layer 24 that overlie the optoelectronic components 26 and 28, but maintains the material in the low-lying regions where the optical waveguides will be defined. The polishing step often reduces the thickness of layer 24 in the low lying areas, particular when the thickness of the initially-formed and cured layer is greater than the thicknesses of the optoelectronic devices.

Planarity is defined with respect a flat (or sometimes gradually bowed) geometrical plane which spans a localized area and which goes through the median height, or average height, of the surface topology in that area. Planarity is a measurement of variance of the surface topology from the geometric plane. The measurement may be mathematically defined in a number of ways, the most typical (and easiest) measurement is the maximum height variation from the geometric plane within the localized area. Sometimes the underlying base substrate 12 may have a slightly bowed surface, and therefore will not be perfectly flat. In this case, the notion of planarity may still be applied by using a geometric plane which has a bowed surface

which follows the contour of the underlying substrate in the localized area of interest. In the present invention, one generally seeks to achieve a maximum height variation of not more than  $0.5\text{ }\mu\text{m}$  from the geometric plane over a surface area of  $2\text{ cm}$  on a side (*i.e.*,  $4\text{ cm}^2$ )

5 To achieve good local planarity, one may use a soft polishing pad, or a dual pad structure comprising a hard outer pad and a softer underlying pad. The selection of polishing pads is well within the ordinary skill in the art. As mentioned above, tungsten polish-stop layers are used over various components to protect them. In this regard, the effectiveness of tungsten as a polish-stop layer may be increased by adding  
10 phosphoric acid to the slurry, which will not significantly affecting the polishing rates of copper and most polymeric materials. To use phosphoric acid for this purpose, it is added in an amount which lowers the pH of the slurry to a value which is between 2 and 4. As a final note on the polishing step, several "dummy" portions of EO material 626, with the overlying polish-stop layer 627, may be distributed over the surface of  
15 base substrate 12 in areas where there are no optical waveguides or opto-electronic devices located. (Such a dummy portion is shown in the lower left corner of FIG. 20). The dummy portions are never used as active components, but serve to reduce the "dishing" phenomenon of the polishing step by increasing the aggregate surface area of polish-stop layer 627. ("Dishing" is where localized hollows are formed in the surface  
20 by the polishing action due to the lack of nearby polish-stop regions or high spots, the dishing effect is greater for soft pads than for hard pads.)

As the next fabrication step, and as shown in FIG. 15, vias are formed through layer 24 to the vias previously made to the bottom electrodes 27 through layer 21. The via may be formed by etching a via aperture, such as by laser or by plasma etch, and  
25 thereafter filling the aperture with conductive material using any of the filling steps described above with respect to the formation of the vias in layer 21. It may be appreciated that the previous formation of the vias in layer 21 may be delayed until the vias in layer 24 are formed, and that the vias in layers 21 and 24 may be formed at the same time by a single via-formation process. It is also possible to form the vias in



layer 24 before layer 24 is polished, or before layer 24 is cured.

Referring to FIG. 16, the next step is optional and comprises a second polishing step which remove excess conductive material from the top of the vias formed in layer 24. This polishing step is relatively brief, and need not remove all of the excess. As the next step, the polish-stop layer 627, and optionally polish-stop layer 27y, are removed by exposing the layers to a suitable etchant. Tungsten polish-stop layers may be readily removed by hydrogen peroxide, which does not damage copper vias or most polymeric layers. As the next step, the optical waveguides are defined in layer 24. This may be done by removing portions 624 of layer 24 which run along each side of each waveguide, and which border on sides of the opto-electronic devices which are not used as optical inputs. FIG. 19 shows a top plan view of the active substrate 20 before portions 624 of core layer 24 are removed, and FIG. 20 shows a top plan view after the portions 624 are removed to define three optical waveguides 24j-24l shown in the FIG. 20. Portions of layer 21 which underlie the removed portions of layer 24 are seen in FIG. 20. As part of this step, the sections of EO material 626 are patterned a second time to provide the final Y-branch shape for switch device 26. The patterning of layer 24 and the portions of EO material 626 may be done simultaneously with a dry etch process which uses a patterned etch mask disposed over the portions of layer 24 and EO material 626 which are to be retained. Wet etching may also be used. In general, the widths of the EO waveguide section 626 and those of the waveguide 24j-24l are not always the same. If the index of refraction of the EO waveguide section 626 is greater than that of core layer 24 by a substantial amount, as can be the case when a chip of III-V compound, such as gallium-arsenide (GaAs) material, is used for section 626, then it is advisable to make the width of the EO waveguide section larger, or smaller, and to taper its dimensions at those locations where it meets waveguides 24i-24l. This action keeps the beam width of the propagating light properly dimensioned in the two materials of different refractive index, and thereby reduces reflections at the boundaries between the two different materials.

As the next step, layer 23 of cladding material is formed over layer 24 and the

exposed regions of bottom cladding layer 21. This causes the sides of the optical waveguides 24j-24l to be covered with cladding material. The result of this operation is shown in FIG. 17. The cladding material filled the removed portions 624 substantially all of the way to the top, but not completely. There will be small depressions in the surface of layer 23 which overlie the removed portions 624 of layer 24. These depressions are usually gradual and smooth enough that metal lines may be formed across them without breakage. If one wishes to reduce the size of the depressions or eliminate them, the following steps may be undertaken. Referring back to FIGS. 15 and 16, the polish-stop layers are kept in place during the removal of portions 624, and are kept in place when a first layer 23 of cladding material is formed over the surface. This first layer is then polished to planarize it and to expose the polish-stop layers. The polish-stop layers are then removed and a second layer 23 of cladding material is formed over the substrate.

It may be appreciated that the following further variations in the steps of defining the optical waveguides may be practiced. As a first variation, one may dispense with performing the second patterning step of the portions of EO material 626 if the first patterning of EO material 626 uses the final patterned image for the material. The dimensions of the Y-branch shape may be enlarged to account for the possibility of misalignment. The advantage of using the two steps of patterning is that one may achieve perfect alignment between the Y-branch shape of switch device 26 and the optical waveguides 24j-24l by using the second etch step to pattern both EO material 626 and layer 24.

As a second variation, which may be used with the first variation, one may use a core material that is photo-definable (also called "photo-refractive"). Such materials have an initial index of refraction which may be changed upon exposure actinic radiation, which is usually light having a wavelength in the range of 365 nm to 400 nm. Such materials usually increase their indices of refraction when exposed to the actinic radiation. In this case, the material is initially deposited with a low index of refraction, and thereby initially acts as a cladding layer. The layer is then pattern exposed to the

radiation to define the optical waveguides by raising the index of refraction in those areas where the waveguides are to be located. The pattern exposure automatically results in the sides of the waveguides being surrounded by cladding material. When active substrate 20 is completed and is in use as an interconnection device, the optical waveguides usually carry light having a lower wavelength (generally in the range of 600 nm to 1.6  $\mu\text{m}$ ) than that used to define them. The use of a photo-definable core material for layer 24 is easily implemented when EO material 626 has been patterned in its final shape before layer 24 is formed. However, extra processing steps may be added to pattern EO material 626 after the waveguides have been photo-defined. It is also possible that some EO materials may have their compositions modified to provide them with photo-definable characteristics. Examples of photo-definable EO materials are disclosed in U.S. Patent No. 5,541,039 to McFarland, *et al.*, entitled "Method for Forming Optically Active Waveguides". In general, making a material photo-definable can be accomplished by finding a way to change its index of refraction in response to exposure to actinic radiation. The changes may be accomplished by causing chemical changes and/or density changes in the material in response to being exposed to the actinic radiation.

In the core layer coating step shown in FIG. 14, an optional clad layer can be coated on the core layer. After the core layer is cured (partially or fully), the optional cladding layer is coated followed by soft and full curing. If the core layer thickness is a little bit thinner than OE device height (including top electrode), the polished surface can be in the cladding layer. In this case, the optional cladding layer is formed over core layer 24 before the polishing step is preformed. This two-layer approach may improve the interface flatness between core and clad layers, resulting in reduced optical losses. Also, the optical field intensity is slightly lower in the cladding layer, further reducing any interface scattering losses compared to forming a CMP surface at the core/cladding interface. The thickness of the core layer may be selected to be close to or less than the OE device/material height excluding the top metal. In this case, by adjusting the top metal thickness, the optional clad layer thickness can be adjusted. Another approach is to

not perform CMP processing on either the core layer or the top cladding layer. This results in a non-planar surface, which can be planarized, if needed, by forming a planarizing layer over the top cladding layer and then performing CMP processing on the planarizing layer. The planarity of the core layer may also be improved using CVD,  
5 MLD, evaporation polymerization, or other vapor phase deposition methods for the polymer layer formation.

When using a photo-sensitive material, which is hardened by light exposure, CMP is not always necessary. After the step shown in FIG. 14, waveguide patterning can simply be carried out by patterned light exposure if the core layer was coated in an  
10 appropriate thickness, that is, close to or less than the OE device/material height excluding the top metal. Further planarization layers and processing steps may be applied after the overcladding layer is formed, if necessary.

Referring to FIG. 18, the last steps are to form vias through cladding layer 23, and to form the top electrodes 27 for switches 26, electrical traces 30, and  
15 interconnection pads 32. Via apertures may be formed in layer 23 in any number of conventional ways, either before or after layer 23 is cured (if it requires curing). Such methods includes laser drilling and wet or dry etching using a photo-lithographical defined etch mask. Once the via apertures are formed, the vias may be filled with conductive material by any of the convention filling methods described above. Metals  
20 are preferred for the conductive materials, with copper being one of the more preferred metals. In order to reduce processing steps, it is preferred to use sputter deposition or blanket electroplating (with a sputtered seed layer) so as to cover the whole surface of layer 23 with conductive material. By performing a blanket coating, one can then use a subsequent etching step to define the electrical traces 30 and pads 32 by an etching step  
25 using a photo-lithographically defined etch mask. The etch mask covers the vias to protect them during the etching step. As an alternative, one can sputter a seed layer over the entire surface of layer 23 and the via apertures. By conventional photo-lithographic steps, one can then form a plating mask over those area where vias, traces, and pads are not to be formed. As a result, the exposed portion of the seed layer

overlies the locations of the vias, traces, and pads, and these exposed portions may them be plated to form the vias, traces, and pads. After plating, the plating mask is removed and a brief blanket etch is performed to remove the portions of the seed layer which were previously covered by the plating mask. As is known in the art, whenever one forms a metal layer over a polymeric layer, it is advisable to first sputter an adhesion layer over the polymeric layer before forming the metal layer. A 200 Å to 400 Å thick layer of chromium may be used for this purpose. The adhesion layer bonds well to both the metal and the polymeric material.

With a few additional processing steps, one may incorporate a VCSEL device 36b' shown in FIG. 9 in the above fabrication step. First, before cladding layer 21 is formed, adhesion layer 25a is formed over base substrate 12, and the VCSEL device is adhere to layer 25a. Before being adhered to layer 25a, the top surface of the VCSEL device with ELO is coated with a polish-stop layer, such as 0.1  $\mu$  to 1  $\mu$ m of tungsten. Layer 25a is soft-baked, and then cured. (Instead of adhering the device to layer 25a, and as previously described, a metal layer may be deposited on the bottom surface of the VCSEL device and the device may be adhered to a metal pad formed on the surface of substrate 12 by various metal bonding processes.) Material layer 25b is then formed over layer 25a. If material layer 25b comprises a fluidized polymeric material, it is soft-baked and then cured. The process substrate is then polished to remove the portion of layer 25b that overlies the VCSEL device. The (tungsten) polish-stop layer protects the VCSEL device during this polishing step. After the polishing step, the polish-stop layer is removed. The manufacturing steps then proceed as indicated above, starting with the formation of cladding layer 21. Mirror 639 (FIG. 9) may be formed any time after layer 24 is formed, and is usually formed after layer 23 is formed. As indicated above in greater detail, the mirror is formed by making a 45° angle cut through layer 24 in region overlying the emitting element 638, and then forming a layer of reflective metal or reflective material. Since the same basic processing steps used to integrate VCSELs and mirrors may also be used to fabricate vertical-type photodetectors, it is preferably to also fabricated vertical-type photodetectors in the above-described

example.

In the above construction examples, the individual components have been adhered to cladding layer 21 (or layer 25a for a VCSEL device) in the face up-position. However, these individual components may be placed in the face down position with the following modifications. In the case of component 28, layer 27 may be patterned to include connection pads for component 28, and component 28 may have its electrode connected to these pads by metal diffusion bonding. Prior to this, cladding layer 21 would be patterned to expose these contacts in bottom layer 27. Once component 28 has been so joined, a high-temperature underfill material may be dispensed under it to prevent air pockets. Vias are then made to the traces in layer 27 to complete the electrical connection of component 28. The formation of such vias was previously described above.

Placing the component 28 face down onto the substrate has the following advantage when component 28 has been formed by the above described epitaxial lift-off process: that is the AlGaAs etch step used to remove the components from the GaAs wafer may be delayed until the components are placed face down on cladding layer 21. After placement on substrate 412, the AlAs etch step is performed to separate the bulk GaAs substrate from the epitaxial layer which contains the components. Thus, one does not need a polymer film, glass substrate, or other substrates to support the opto-electronic components during the placement steps since the GaAs bulk substrate provides this function. It may be appreciated that a whole GaAs wafer may be placed face down on cladding layer 21, or that the GaAs substrate may be first diced to separate the individual components from one another. For VCSEL devices, these steps are performed with layer 25a and a metal layer formed underneath layer 25b.

Another process for the integration of thin film device integration with waveguides is shown in FIGS. 74-81. As shown in FIG. 74, an epitaxial waveguide OE layer is grown on a GaAs substrate, metallized, and patterned to define a plurality of OE devices 620. The GaAs waveguide core layer may comprise a p-i-n waveguide core layer with abrupt index changes but preferably has a tapered refractive index (*e.g.*, core shaped along the light propagation direction) such as that used for a spot-size conversion laser

diode. The epitaxial films can be electro-absorption (EA) light modulator, Electro-Optic (EO) light modulator, photodetector, optical gate device, optical switching wavelength filter, tunable filter, wavelength filter, wavelength converter, *etc.*, by using multiple quantum well or quantum dot structures. A metal contact layer is deposited on the surface, along with a Au contact film and, if necessary, a surface film of tungsten to stop CMP in later processing steps). The top electrodes and epitaxial layer are then patterned using conventional patterning techniques.

As shown in FIG. 75, the epitaxial thin-films with devices 620 are transferred to a supporting transfer substrate (glass, quartz, mylar, or any other substrates) by epitaxial liftoff (ELO). The adhesion between the ELO films and the supporting substrate can be made by, for example, Vaseline or black wax or an adhesive such as epoxy, polyimide, bonding sheet, thermo-plastics, underfill material, or conductive adhesive.

As shown in FIG. 76, after the semiconductor substrate is lifted off, the ELO devices 620 are transferred onto an under-clad layer 21 disposed on a substrate 12 which may comprise glass, quartz, Si, Al, AlN, or a variety of other substrate materials. The ELO devices 620 can be attached to the underclad layer 21 by several well-known mechanisms, including Van der Waals forces and adhesives bonding. If metal pads are formed on the cladding layer, diffusion bonding, solder bonding, transient liquid bonding (TLB), wire interconnect technology (WIT) can be used for attaching the ELO devices 620. In this case, the ELO device surfaces may also be coated by metal also, such as shown in an example described below with respect to FIGS. 82-89.

In order to form a three-dimensional waveguide that is optically coupled to the p-i-n waveguide of the ELO segments, core layer 24 and clad layer 23 are successively formed using the above-described liquid polymer coating steps, as shown in FIG. 77. It is desirable to adjust the core thickness be close to or less than the p-i-n semiconductor film thickness so that there is strong optical coupling to the p-i-n core layer. However, slight non-uniformities and/or perturbation in core thickness near the edge of the ELO segments will not significantly degrade the efficiency of light propagation. By using vapor phase deposition such as CVD, MLD, evaporation polymerization, the perturbation

strength (i.e., non-uniformities) can also be reduced. If necessary, the surface of the deposited core layer 24 is planarized by CMP to improve its smoothness and uniformity. The CMP can be automatically stopped by a tungsten (W) film on the top of the ELO devices 620.

5           As indicated in FIG. 77, an upper cladding layer 23 can also be coated on the core layer 24. This has several benefits. One benefit is that it permits the core layer to be equal to or even slightly thinner than the OE device height, permitting greater design freedom and/or design freedom. Additionally, it may result in lower waveguide losses because the cladding layer 23 can be polished to a surface that has a more uniform  
10       interface with reduced optical scattering losses (e.g., a comparatively thick cladding layer deposited over a core layer 24 may be readily polished back to an optically smooth surface. Moreover, since the optical field strength is typically lower in the cladding layer 23 than in the core layer 24, optical losses at a polished surface in the cladding layer may be reduced compared to the case that the CMP polish surface is at the core/cladding  
15       interface). After the core layer 24 is cured, the optional upper cladding layer 23 is coated followed by soft and full curing. A partial cure of the core layer 24 is desirable because it can increase the adhesion strength between the core and clad layer.

          As shown in FIG. 78, the core layer 24 is patterned into longitudinal waveguides and then another cladding layer 23' is formed around the longitudinal waveguides, as  
20       shown in FIG. 79. Vias and electrodes 27 are formed to the the EO devices 620, as shown in FIG. 80, followed by removal of the undercladding substrate 12 and back-side processing is applied to make bottom electrodes 27 and vias, as shown in FIG. 81. However, if metallization of the substrate and under clad layer 21 is done before the thin-film device attachment, the substrate removal and back-side processing is not necessary.  
25       The active layer can be attached to another layer or substrate before removing the substrate. This is preferably for dimensional stability. If necessary, a buffer polymer layer 613 can be inserted between the substrate and cladding layer, and the metallization can be applied onto the buffer layer 613 and to the cladding layer, as is done in the embodiment shown by FIGS. 82-89 below. Device dividing is performed after ELO and



metal coating.

FIG. 82-89 show another variation in which the core layer thickness is thinner than the device thickness to reduce light scattering by the electrodes of the device. The ELO devices 620' are attached on pads formed on substrate 12, as shown in FIG. 84, which in turn are formed on a buffer layer 613 and dielectric spacing layer 614. Then, the cladding layer 21 is formed with the devices 620' in place, and then the core layer 24 is formed. The resulting structure is shown in FIG. 85). Some distortion may result in the core layer 24 in a short region disposed around the edge of each ELO device 620'. However, while this may cause some optical losses, the total optical losses will be small because of the short scattering length. To address this, CVD, MLD, evaporation polymerization, or other vapor phase deposition methods may be used in the embodiment of FIG. 82-89 prior to forming the core to improve the smoothness of the core layer.

Next, as shown in FIG. 86, the core layer 24 is patterned using any of the methods described above, followed by the over-coating of clad layer 23, as shown in FIG. 87. Vias and electrodes are formed as described above, which are shown in FIG. 88. The device is removed from substrate 12 and attached to an appropriate component, as shown in FIG. 89.

As indicated in the discussion of FIGS. 74-81 and 82-89, the core thickness of the active device ELO segment is preferably thinner than that of other portions. This permits a high electric field strength to be obtained at a low operating voltage. Furthermore, by reducing the ELO optical core width, as shown in FIG. 67, the capacitance is reduced. This facilitates high-speed device operation.

While FIGS. 81 and 89 show vias connected to ELO electrodes, other connection methods may also be used. In particular, direct formation of electrodes connected to the E/O electrodes is another possibility.

There are many potential variations of the above described process. Referring back to FIGS. 77-79, when photo-sensitive material, which is hardened by light exposure, is used, CMP is not always necessary. Consequently, after coating the core layer, waveguide patterning can simply be carried out by light pattern exposure if the core layer

was coated in an appropriate thickness. Planarization may be applied after overladding layer is formed, if necessary. The metallization sequence may also be varied. For example, by depositing a ~3000 Å thick W film on the clad surface before CMP, CMP can be performed using the W film as a CMP stop layer. In this case, the W film on the Au is unnecessary.

While one ELO technique has been discussed in detail, the present invention may be applied to any optical material or device which may be selectively lifted off from the substrate upon which it was deposited or formed. ELO can be done by GaAs substrate etching with  $\text{Al}_{1-x}\text{Ga}_x\text{As}$  etch-stop, or using AlAs etchable layer. However, the Semiconductor substrate is not restricted to GaAs. InGaAsP-related epitaxial films can also be used for wavelength of ~1.3  $\mu\text{m}$  and ~1.5  $\mu\text{m}$  applications. Other materials may also be lifted off. For example, a large refractive index film, like  $\text{TiO}_2$ ,  $\text{WO}_3$ ,  $\text{SiN}_x$ , Si etc. film can be deposited on substrates, such as Si, metal, or polymer, which may be selectively etched away, permitting these film to be embedded in the manner of the present invention. Thus, the teachings of the present invention may be applied to a wide variety of thin-film materials and devices. As one example, if a rare-metal-doped glass film is embedded, then it may act as an optical amplifier. Organic or inorganic functional films such as luminescent films, photo-refractive films, or nonlinear optical films may also be embedded. Optical delay lines comprised of high refractive index materials may similarly be embedded. The present invention thus provides a versatile way to optically integrate a variety of optical components. For example, resistors, capacitors, amplifier chips, driver chips may also be embedded. In the case of electronic elements fabricated on a silicon chip, polishing may be effective to reduce the thickness of the chip instead of ELO. The attachment of the ELO film may also include a variety of materials and processes, such as metal diffusion, AuSn bonding, Pd bonding, or solder process, WIT, TLB etc. as well as adhesive process.

All the processes and structures mentioned in the present disclosure can be applied to matrix optical switches, including wavelength switching, for XBAR switching by connecting a plurality of switch parts of transferred thin-films by polymer waveguides

in a network configuration. The switching elements may comprise: internal total reflection switches, Mach-Zehnder switches, digital switches, directional couplers, and optical gate devices based on semiconductor optical amplifier, wavelength filter, or tunable filter. The method of the present invention may thus be used to realize an active substrate with a matrix optical switch function.

### **DISCUSSION OF FIGS. 21-30**

The above active-substrate construction may be extended in many ways to construct more complex optical-electrical interconnect systems. For example, as shown in FIG. 21, the active substrates 20 described above may be horizontally attached to a backplane (or motherboard) 100, which comprises its own optical substrate 120, which is similar in construction to active substrate 20, and which may be constructed by the previously described steps. As another example, the active substrates 20 described above may be vertically attached to a backplane (or motherboard) 210, as shown in FIGS. 31-32. As yet another approach, the active substrates may be stack upon on another with interleaving "layer" of integrated circuit chips between them, as shown in FIGS. 34-36, 71, and 109-111.

Referring to FIG. 21, the horizontal attachment of the active substrates 20 to a backplane (or motherboard) 100 is first described. Backplane (motherboard) 100 comprises an active substrate layer 120 having a plurality of optical waveguides 124a - 124h formed therein using a bottom cladding layer 121, a patterned defined core layer 124, and a top cladding layer 123, which can be seen in FIG. 22. For the purposes of illustration, and without loss of generality, backplane (motherboard) 100 houses four identical MCM-type active substrates 20, each of which houses four IC chips. In order to show the routing of the optical waveguides 124, two of the four active substrates 20 shown in FIG. 21 have been detached and are not shown in the figure. Backplane (motherboard) 100 comprises a plurality of vertical optical couplers (154, 156, 160) for transmitting and receiving optical signals to the MCM active substrates 20, and each of the MCM active substrates 20 previously described have been modified to replace their

V-groove optical connectors 13-15 with corresponding vertical optical couplers 44 and 48. These modifications are described below after a general description of backplane (or motherboard) 100 has been given.

5 The positions of the waveguides and vertical couplers underneath the upper-left and upper-right MCM substrates 20 are the same as those underneath the lower-left and lower right MCM substrates 20. This is done to give the reader a view of backplane (motherboard) 100 in the cases when the substrates 20 are mounted (upper-left and upper-right positions) and when they are not mounted (lower-left and lower-right positions).

10 A source of light for backplane (motherboard) 100 is generated by an emitter device 136, which may be any of the light emitting devices 136 described above and illustrated in FIGS. 6-10. The output of emitter device 136 is coupled to waveguide 124a, which is routed to up to a location which adjacent to the upper-left MCM substrate 20. From this point, waveguide 124a is gradually bent in a 90° angle and is routed underneath the upper-left MCM substrate 20, and extended to pass underneath the upper  
15 right MCM substrate 20. Between emitter device 136 and the upper left MCM substrate 20, waveguide 124a passed through a horizontal beam splitter 164, which divides off a portion of the light (e.g., 50%) to waveguide 124b, which meets waveguide 124a at a right angle. The construction of horizontal beam splitter 164 is described below in greater detail after the general description of backplane (motherboard) 100. Waveguide  
20 124b is routed to the location where the lower-left MCM substrate 20 will be placed, and further over to the location where the lower-right MCM substrate 20 will be placed. Under each location for the MCM substrates, waveguide 124b passed through a vertical beam-splitter 154, which directs a portion of the light upward toward the MCM substrate 20, where it is coupled into a waveguide 24a by a receiving vertical coupler 44 (shown in  
25 FIG. 22). The constructions of vertical beam splitter 154 and receiving vertical coupler 44 are described below in greater detail after the general description of backplane (motherboard) 100.

Waveguide 124c conveys an optical signal between the lower-left MCM substrate 20 and the lower-right MCM substrate 20. To receive the optical signal from the lower-

left MCM substrate, backplane (motherboard) 100 comprises a receiving vertical coupler 160 under the terminal end of the waveguide 24h of the MCM substrate. The light signal from the lower-left MCM substrate 20 is transmitted vertically toward the surface of backplane (motherboard) 100 by a transmitting vertical coupler 48. This light is received  
5 by a receiving vertical coupler 160 of backplane (motherboard) 100, which bends the light by 90° and directs it into waveguide 124c. Waveguide 124c conveys the optical signal to a transmitting vertical coupler 156, which is positioned underneath the lower-right MCM substrate 20. Coupler 156 bends the optical signal by 90° and directs it vertically upward into a receiving vertical coupler 44 of the lower-right MCM substrate  
10 20. Coupler 44 receives the light, bends it 90° and directs it horizontally into waveguide 24g of substrate 20. The constructions of vertical couplers 44, 48, 156 and 160 are described below in greater detail after the general description of backplane (motherboard) 100. Waveguide 124e is configured similarly to waveguide 124c and it conveys an optical signal from the upper-left MCM substrate 20 to the upper-right MCM substrate 20  
15 in a similar manner using a similar configuration of vertical couplers.

Waveguide 124d is coupled to an optical fiber 102 at one of its ends by a conventional V-groove connector 112, and receives an optical signal on fiber 102 from an outside source. Waveguide 124d is coupled to a second receiving vertical coupler 156 at its other end, and the second vertical coupler 156 directs the optical signal upward into a  
20 receiving vertical coupler 44 of the lower-left MCM substrate 20. This vertical coupler 44 directs the optical signal into waveguide 24g of the lower-left MCM substrate 20. Optical waveguide 124f is similarly coupled to an optical fiber 103 by a V-groove connector 113 at one of its ends, and a third vertical coupler 156 at its other end. Waveguide 124f receives an outside signal from an optical fiber 103.

25 Waveguide 124g is coupled to a second receiving vertical coupler 160 at one of its ends. This receiving vertical coupler 160 receives an optical signal from the lower-right MCM substrate 20 and directs it into waveguide 124g. The other end of waveguide 124g is coupled to an optical fiber 104 by a conventional V-groove connector 114, and the optical signal in waveguide 124g is conveyed as an output signal of backplane

(motherboard) 100. Optical waveguide 124h is similarly coupled to a third receiving vertical coupler 160 (not shown in FIG. 21 but underneath the upper-right MCM substrate 20) and an optical fiber 105 through a V-groove connector 115. Waveguide 124h conveys an output signal from the upper-right MCM substrate to optical fiber 105.

5           Power supply voltages may be conveyed from backplane (motherboard) 100 to the MCM active substrates 20 by conductive pads 151 and 152, as shown in FIG. 21. The power may be distributed in backplane (motherboard) 100 by conductive layers within active substrate 120. Active MCM substrates 20 are augmented to have corresponding power pads for coupling to pads 151 and 152. Backplane (motherboard) 100 may have electrical traces for conveying electrical signals between MCM modules. These electrical traces may be formed in dielectrically-isolated conductive layers with vias being formed to respective connection pads.

10           Instead of using optical fibers to convey optical signals to and from the MCM module or backplane (motherboard), one may use what we call "film waveguide arrays" or simply "waveguide arrays". Such a waveguide comprises a thin flexible sheet of polymer material having plurality of optical waveguides surrounded by cladding material, and usually having vertical couplers at one or both ends of the waveguides. One edge of the waveguide array is adhered to an area of the active layer 120 in such a way that its vertical couplers in its edge are aligned with corresponding vertical couplers in layer 120. 15           Fiber array or imaging guides are also useful. The optical power supply 136 may be placed on the OE-MCM side, or it may be supplied by an external light source. In the latter case, the active substrate of backplane 120 may only have waveguides, mirrors, and grating reflectors and no OE devices.

20           Having generally described the structure of backplane (motherboard) 100, the constructions of the beam splitters and vertical couplers of backplane (motherboard) 100 and MCM substrates 20 are now described with reference to FIGS. 22-26. In reviewing these figures, it will be seen that the underlying base substrates 12 has been removed from active substrates 20, which enables better optical coupling of the optical signals between backplane (motherboard) 100 and active substrates 20. Base substrate 12 may

comprise aluminum or silicon, quartz, glass or other removable substrate materials, for example, and may be removed by etching or other removal methods. Other etchable metals and materials may be used. In this case, a protective etch stop layer may be disposed between base substrate 12 and active substrate 20. In addition, substrate release techniques, such as those described in U.S. patent No. 5,258,236 to Arjavalasingam *et al.*, may be used to separate base substrate 12 from active substrate 20. These methods typically use a transparent substrate, a polymeric release layer that can be ablated by a laser beam directed through the transparent substrate, and a reflective metal layer formed over the polymeric release layer to protect active substrate 20 from the laser beam.

Another approach is to use a silicon wafer with a thick aluminum top layer as substrate 12, and then laterally etch the aluminum layer from the sides of the wafer (with a protective coating on the top surface of active substrate 20) to separate active substrate 20 from the silicon wafer.

FIG. 22 shows a cross-sectional view of backplane (motherboard) 100 and the upper-left MCM substrate 20 in the region of vertical beam splitter 154 of backplane (motherboard) 100 and receiving vertical coupler 44 of substrate 20. Backplane (motherboard) 100 comprises a base substrate 12, a conductive layer 151 for providing one potential of the power supply ( $V_C$  or ground), a bottom cladding layer 121, a core layer 124, a top cladding layer 123, and a second conductive layer 152 for providing a second potential of the power supply (ground or  $V_C$ ). Layers 121, 123, and 124 may comprise the same materials as layers 21, 23, and 24, respectively, as previously described above. Also, in some cases, materials which have lower thermal stability (*e.g.*, cannot withstand high processing temperatures like epoxy, acrylate, *etc.*) but which have lower optical propagation losses compared to layers 21, 23, and 24 may be used for layers 121, 123, and 124. Vertical beam splitter 154 is formed in the path of waveguide 124b, and comprises an optical grating structure 155, which may have a variety of configurations, as is well known in the art. Grating 155 comprises a periodic structure of optical material having an index of refraction which is different from that of waveguide 124b (either higher or lower). When incident light strikes the material of grating 155, a

portion of the light is reflected from the surface of grating 155 to a vertical direction and a portion is transmitted through grating 155, with the ratio of the reflected and transmitted portions being dependent upon the difference between the indices of refraction of the materials of grating 155 and the core material 124, and upon the number of periods in the grating. To achieve a 90° angle between the incident light and the reflect light, at least a portion of surface of grating 155 is angled at or near 45° with respect to the path of optical waveguide 124b. The gratings 155 are spaced such that the reflections from their surfaces are nearly in phase so that the reflections from the individual gratings constructively add to build the light beam that is transmitted to active substrate 20. (The spacing is usually on the order of one wavelength of light, as measured in the materials 124 and 155). U.S. patent No. 5,116,461 to Leiby, *et al.* Discloses a method for etching 45° angle trenches in polymeric material for the purpose of fabricating such grating structures. Once formed, the etched structures may be filled with material having a different index of refraction. The fractional amount of light that is reflected upwards is a function of the number of gratings and the difference in the indices of refraction, and can be computed using optical analysis known to those of ordinary skill in the art.

Any number of the known grating structures may be used, and the gratings 155 do not need to extend through the entire height of waveguide 124b. If waveguide 124b is formed from a photosensitive core material, portions of it corresponding to grating portions 155 may be removed by photo exposure using an interference pattern, such as that generated by holographic means. In a similar manner, such an exposure may be used with a photo-refractive core material. In addition, other types of periodic grating structures may be used, such as that described by U.S. patent No. 4,806,454. Alternately, instead of using a grating a semi-transparent mirror (e.g., a metal mirror whose thickness and/or composition is selected to achieve a controlled reflectivity) or a multi-layer dielectric filter may also be used instead of a grating to perform the same function of vertically reflecting a fraction of the light upwards.

The portion of light reflected vertically from grating 155 pass through a ball of optical "glue" material 153 to substrate 20. The optical glue has an index of refraction



which is relatively close to that of core materials 124 and 24 (*e.g.*, much closer the indices of the waveguides than the index of air,  $n=1$ ). The optical glue improves transmission efficiency between backplane (motherboard) 100 and active substrate 20 by reducing the magnitudes of reflected waves. Exemplary glues are disclosed by Norio Murata in an article entitled "Adhesives for Optical Devices", the 48<sup>th</sup> conference of the Electronic Components and Technology Conference (ECTC, May 1998). Polyimide material can also be used. One may also form photo-refractive glues based on the photo-refractive compositions disclosed in Japanese published patent applications JP 9-157352, JP 9-090153, JP 8-320422, 7-077637 and European patent publication EP-689,067-A , which are assigned to the assignee of the present application. The self-focusing beam effect (SOLNET) described in our European patent application EP-689,067 may be used to form a vertical waveguide in the body of optical "glue" disposed between the substrates. In this process, the portion of material through which a light beam is first passed through has its index of refraction raised by the light beam, which then causes this material to be a core material while the remainder of the material serves as a cladding material. This creates a self-aligned vertical optical waveguide. The initial beam of light may be provided through one of the waveguides, or it may be provided by an external application of a writing light beam directed from one side of the optical joint. In addition, it is effective to provide light from both waveguides, or beams from both sides of the optical junction.

In addition to these possibilities, one may use many conventional bonding sheets or underfill materials to improve the optical coupling (over the case where there is no material between substrates) since these materials will have indices of refraction which are relatively close to that of the waveguides.

Vertical coupler 44 of active substrate 20 is constructed in a similar as the optical waveguide which is coupled to the output of a VCSEL device previously described and illustrated with respect to FIG. 9. An optical via 45 is formed through layers 25a, 25b, and cladding layer 21 by forming an aperture in these layers by laser drilling, laser ablation, or plasma etching (preferably after they have been cured), and then filling them

with core material, usually when layer 24 is formed. Then, mirror structure is formed by forming a bevel surface on the waveguide as previously described, and thereafter forming a layer of reflective metal or reflective material over the beveled surface. In some cases, the optical vias are not needed, such as when the optical absorption coefficients of layers 25a and 25b are sufficiently low. An anti-reflection (AR) coating may be deposited on the surfaces of the substrate to reduce reflection of light.

FIG. 23 shows a cross-sectional view of backplane (motherboard) 100 and the upper-right MCM active substrate 20 in the region of where optical waveguide 124e meets a vertical coupler 156. The vertical coupler 156 comprises a layer 158 of reflective metal formed on a beveled edge of a portion 157 of a material layer. The bevel may be formed by laser ablation (with the laser at a 45° angle tilt to the material layer), by laser assisted plasma etching (again with the laser as a 45° angle tilt, see for example U.S. patent No. 5,116,461), by plasma etching with a tilted substrate, ordinary plasma etching with a tapered mask, or tilted lithographic exposure (see for example Japanese patent JP 96-262265). A preferred laser ablation method for forming beveled cuts is described in greater detail below with respect to FIGS. 90-101.

Vertical coupler 156 can be formed *in-situ* and can be incorporated in the processing steps for forming active substrate 20 previously described above and illustrated in FIGS. 11-18. Such exemplary steps are provided below after the other optical couplers are described.

FIG. 24 shows a cross-sectional view of backplane (motherboard) 100 and the upper-left MCM active substrate 20 in the region of where optical waveguide 24h of the active substrate 20 terminates in a transmitting vertical coupler 48, which is over a receiving vertical coupler 160 of backplane (motherboard) 100. Transmitting vertical coupler 48 has the same construction as receiving vertical coupler 44 shown in FIG. 23, except for the orientation of the mirror layer 46. Receiving vertical coupler 160 has the same construction as transmitting vertical coupler 156 shown in FIG. 23, except for the orientation of mirror layer 158. It is also noted that instead of using couplers 156 and 158 on the backplane (motherboard) side, one may use couplers 44 and 48 on the backplane

(motherboard).

It is noted that the grating structure of vertical beam-splitter 154 may be used in place of any of vertical couplers 156, 160, 44, and 48, with an appropriate orientation of the gratings 155. In these structures, the reflected light may be increased over the transmitted light by selecting materials that have a large difference in their indices of refraction. Alternately, to achieve complete reflection, a mirror can be used instead of beam-splitter 154.

FIG. 25 shows a top plan view of horizontal beam-splitter 164, and FIG. 26 shows a cross-sectional view thereof. Its construction is similar to that of vertical beam-splitter 154 except that the gratings are placed in a different orientation, as shown at 165. Gratings 165 are easier to form than gratings 155 since gratings 165 are not tilted with respect to the surface of core layer 124. A simple anisotropic plasma etch or laser ablation of core layer 124 using a metal or photoresist mask (plasma etch only) or dielectric multilayer mirror (laser ablation only) may be used to form the apertures for gratings 165.

#### **Description of FIGS. 90-108**

A preferred laser ablation method for forming a beveled cut using a laser tilted at a  $45^\circ$  tilt angle impinging upon a shadow mask is shown in FIGS. 90-101. The preferred bevel cut method permits beveled mirrors to be fabricated which may be aligned to any preferred waveguide orientation. Moreover, the preferred bevel cut method permits different bevel cut orientations to be patterned on the same wafer.

In a first step, as shown in FIG. 90, a metal or dielectric ablation mask layer 810 is deposited on a polymer waveguide substrate 20 having cladding and core sub-layers, and optionally other components described herein. The ablation mask layer 810 is lithographically patterned with apertures 811 where all of the mirrors will eventually be formed. To reduce the number of lithographic patterning steps required, additional metal shadow masks 820-1, 820-2, 820-3, and 820-4 are used to select which apertures are ablated at a particular cut orientation. The shadow masks 820 preferably block, or

obscure, a fraction of the apertures 811. Preferably, the shadow masks 820 have apertures 821 slightly larger than the lithographic apertures 811 which are to be ablated in a particular ablation step. A shadow mask 820 may be in direct contact with the wafer surface or placed slightly above the wafer surface.

5           To form a first bevel cut step, a metal shadow mask 820-1 is placed over the wafer to protect a desired fraction of the lithographically patterned apertures 811 from exposure. Referring to FIG. 91, the substrate 20 and laser 830 are oriented with respect to one another so that one edge of each exposed lithographic aperture 811 is uniformly shadowed by the ablation mask 810 during exposure of the polymer layer by the excimer  
10   laser beam 830 whereas the opposite edge of the aperture is undercut. That is to say, in the aperture of an exposed ablation mask a profile of constant illumination intensity as a function of depth in the trench forms a parallelepiped shaped region wherein the tilt of the parallelepiped relative to the surface normal of the trench is a function of the tilt angle of the laser. To form mirror surfaces, the substrate 20 and laser beam 830 are oriented at  
15   angle with respect to one another, including refraction and diffraction effects, to form aperture sidewalls which have an angle of approximately forty-five degree ( $45^\circ$ ) relative to the surface normal of the bottom of the waveguides (i.e., the top and bottom surface of the waveguides). The laser beam is scanned over the surface of shadow mask and substrate, such as by moving the laser beam or the substrate, or by a combination of  
20   moving both. We have called this scanning method "moving neon ablation", or NMA, method, although other types of lasers may be used. The laser exposure forms a parallelepiped-shaped trenches 840 in non-shadowed apertures with a forty-five degree side-wall angle on two of the walls as a consequence of the shadowing effect of lithographic mask layer 811, as shown at 840-1 in FIG. 92 where shadow mask 820-1 has  
25   been removed. The process may be repeated by placing changing the orientation angle between the surface normal of substrate 20 and laser 830, placing a second shadow mask over the surface to expose other apertures and then appropriately orienting the sample in another direction. (To distinguish these directions in the figures, we has assigned four directions 1-4 at the edges of the substrate.) For example, in order to form beveled cuts

on the other two side walls, the sample may be rotated ninety degrees while keeping laser 830 fixed (as shown in FIG. 93, and then exposed again using a different shadow mask 830-2, as shown in FIG. 94. The resulting angled trench is shown at 840-2 in FIG. 95. By repeating the process, mirror surfaces with an arbitrary cut orientation and positions may be formed. This is shown by FIGS. 96-101, where two additional ablation steps using two additional shadow masks 820-3 and 820-4 are shown with corresponding trenches 840-3 and 840-4.

The same ablation process may be modified to obtain vertical sidewalls as well. Orientating the beam normal to the surface of the ablation mask will result in no shadowing. Consequently, the laser light will enter the aperture at a normal angle. This is shown in FIGS. 102-104, where shadow mask 820-4 has been used to form vertical sidewall cuts rather than angled sidewall cuts.

As is known in the field of integrated optics, vertical sidewalls may be used to form reflective surfaces to deflect a waveguide mode into another co-planar waveguide formed from the same active layers but oriented along a different direction, as shown in FIGS. 105 and 106, which are top plan and cross-sectional views of a corner turning mirror 850. This is useful, for example, in forming corner turning mirrors in a which a forty-five degree reflective surface is used to horizontally deflect the waveguide mode by a reflection angle of ninety degrees. As is well known in the field of integrated optics, the efficiency of a corner-turning mirror is strongly dependent upon how vertical the mirror surface is. A mirror surface that deviates even a few degrees from a true vertical surface has a significantly reduced efficiency. Thus, while RIE may be used to form a corner turning mirror, a laser ablation method is a preferred method because of its potentially smoother and more vertical mirror surfaces.

Referring to FIG. 105, light in a first waveguide section 851 reflects against a forty-five degree mirror surface 850 into a second perpendicular waveguide 852. The mirror preferably comprises a portion of the waveguide that is etched normal to the wafer surface. The etched surface is preferably etched all of the way through the core layer 24 and cladding layer 23 in order to achieve substantially complete reflection of light from

first waveguide section 851 to second waveguide section 852. However, if less than complete reflection is desired, the mirror may only be partially etched through the outer cladding so that the effective reflection coefficient is reduced. As shown in FIG. 106, after the polymer cladding and core layers 23 and 24 are ablated, the side walls may also  
5 be coated by a reflective metal mirror surface 853, followed by deposition of the overcladding layer. The substrate may later be removed, if necessary.

A variety of different mask structures may used in a laser ablation process. In addition to a metal mask, a reflective multi-layer dielectric mask, may also be used. A multi-layer dielectric mask may comprise materials with a low optical absorption at  
10 excimer laser frequencies. Additionally, the dielectric constants and layer thickness of a multi-layer dielectric may be selected so that the mask efficiently reflects light at the excimer laser frequency. Generally, any mask that ablates at a significantly slower rate than the polymer layer may be used. A multi-layer dielectric lithograph mask is preferable, since its can be relatively thin, thus improving edge resolution. A laser  
15 ablation process preferably includes means to translate the beam relative to the sample to expose an large area. Any common technique may be used for this purpose, such as a movable stage or optics to scan the beam. While an excimer laser is a preferred laser, other ultraviolet lasers, such as the THG-YAG or FHG-YAG laser may also be used. An ablation gas, such as He, can be used for the carrier.

20 Many of the same principles may be used in a reactive ion etching (RIE) process. An RIE mask may be deposited and patterned on the surface of the substrate to form apertures. Additional shadow mask may then be used to protect some of the apertures from RIE. Directional RIE at oblique angles has ions impinging upon a substrate. Shadowing of ions will occur in a similar manner from a mask, thereby producing tilted  
25 sidewalls. Thus, the above process in FIGS. 90-104 may be repeated using an RIE process in place of a laser beam.

FIGS. 107 and 108 are top plan and cross-sectional views of another embodiment of a waveguide coupler with forty-five degree waveguide mirrors. A waveguide cladding layer 21, such as Fluorinated polyimide, is first deposited on a removable substrate, such

as an Aluminum substrate. The core layer 24 is then deposited. The core layer 24 is patterned into waveguides. An overlaid layer 23 is deposited over the patterned core layer 24. The core layer 24 and clad layers are then patterned using RIE or laser ablation to form mirror/coupler surfaces. The surfaces are then metalized, as shown at 853. The substrate is then removed. The substrate removal can be done after the film is attached to another board or film. Other variations, such as forming electrical contact pads and vias may also be performed before the substrate is removed. Optional buffer and passivation layers may also be added. If desired, the mirror may also be formed after the core layer 24 is formed prior to deposition of the overlaid layer 23.

#### **Description of FIGS. 27-30.**

As mentioned above, the fabrication of vertical couplers 156 and 160 shown in FIGS. 20-26 may be easily incorporated in the fabrication steps for making optical switch 26 previously described above and illustrated in FIGS. 11-18. The additional steps are illustrated with respect to FIGS. 27-30. Referring to FIG. 27, at the same time of forming bottom electrode 27 for switch device 26, a bottom metal patch 159 is formed for the vertical coupler. Metal patch 159 serves as a barrier layer to a subsequent laser drilling, laser ablation, or plasma etching process, and is located mainly where a laser beam in this subsequent etching step will hit layer 121. Next, material layer 157 (the same as layer 626) is formed, and then a top metal mask layer 161 is formed which has apertures where the beveled cuts will be made. A angled etch is then performed to form an angled aperture 162 and the beveled edge for the vertical coupler. The angle etch may be performed by the previously-described steps of laser ablation, moving neon ablation (MNA) (previously described in regards to FIGS. 90-104), laser assisted plasma etching with tilted laser, or by plasma etching with tilted substrates or ordinary plasma etching with a tapered mask, *etc.* Layer 161 acts as etch mask for this step by providing the aperture through which the laser light will pass and strike layer 626 to form the angled trench. In the case of MNA, the second masks are used, and repeated ablation with changing angles may be performed. If the material is photosensitive, the angle cut may

be defined by exposing the substrate to actinic radiation (whose beam direction is tilted with respect to the substrate surface), followed by developing the image. A blanket exposure to actinic radiation may be done since layer 161 acts as a portable conformal mask (PCM). The result of these steps is shown in FIG. 27.

5 Referring to FIG. 28, layer 161 is then removed, and the combined etch-stop/polish-stop layer 627 is formed over the surface of the substrate, as in the previously described process. Next, the mirror metal 158 for the vertical coupler is formed over layer 627, and then both layers are defined simultaneously by a standard pattern etched step through a patterned photoresist layer. The substrate is then subjected to a standard  
10 plasma etching process, as in the previously described method, which selectively etches polymeric material anisotropically. Such plasma etches are well known to the art. The result of these steps is shown in FIG. 28. Next, core layer 124 is formed over the substrate and cured, as shown in FIG. 29. Finally, the structure is polished by chemical mechanically polishing, as in the previously described method. The result is shown in  
15 FIG. 30. Typically, the top-most portions of mirror metal 158 are more easily removed than the polish-stop layer 627. The processing of the substrate then resumes with the previously describe steps after the polishing step (FIG. 15). As an optional step, top cladding layer 123 may have an aperture formed above the beveled mirror section and filled with the same material as core layer 124b. In general, it is not necessary to etch  
20 cladding layer 123 in those locations where the light is reflected vertically from the core material because the exiting light strikes the cladding layer at nearly a  $90^\circ$  angle, which is greater than the critical internal reflection angle. However, there is some amount of reflected light, and corresponding loss of efficiency, when there is a portion of cladding layer above the mirror, and this amount increases as the difference in indices of refraction  
25 increases.

It is desirable to have process variations which reduce the waveguide losses associated with any optical scattering associated with interface roughness at the CMP polishing surface. In the core layer coating step shown in FIG. 29, an optional clad layer can be coated on the core layer in order to improve the interface smoothness proximate to



the core layer. After the core layer is cured (partially or fully), the optional cladding layer is coated followed by soft and full curing. If the core layer thickness is a little bit thinner than OE device height, the polishing plane will lie in the optional cladding layer above the core layer. This two-layer approach may improve the interface flatness between core and clad layer, since the optional cladding layer may be polished to a common plane resulting in a potential reduction in optical scattering losses. Additionally, the polishing plane may lie a significant distance in the cladding layer (e.g., more than a few thousand Angstroms) so that the optical intensity at the polished surface is reduced, further reducing scattering losses. It may thus be preferable to select the thickness of the core layer to be close to or less than the OE device/material height excluding the top metal since this permits the thickness of the optional cladding layer to be determined by the selection of the top metal thickness. Alternately, optical scattering losses may be reduced if the CMP process is applied after over cladding layer formation not after core layer formation. Another approach is to not perform CMP processing on either the core layer or the top cladding layer. This results in a non-planar surface, which can be planarized, if needed, by forming a planarizing layer over the top cladding layer and then performing CMP processing on the planarizing layer.

The fabrication process may also be further modified to eliminate CMP polishing steps which may introduce optical scattering losses at key interfaces. When a photo-sensitive material, which is hardened by light exposure, is used to pattern the waveguides, CMP is not always necessary. After the step shown in FIG. 29, waveguide patterning can be carried out by light pattern exposure if the core layer is coated in an appropriate thickness of a photo-sensitive material, that is, close to or less than the OE device/material height excluding the top metal. Although the patterned waveguide may traverse a portion of the 45-degree-surface of the reflector, this will not significantly interfere with its function in reflecting the guided light. Additional planarization layers may be applied after the overcladding layer is formed, if necessary.

The step of forming the beveled mirror surface may be performed after the top cladding layer is formed over the core layer. In this case, complete reflection is expected

since the evanescent wave can be reflected. That is to say, the mirror surface can be etched through the upper cladding and core layers at least through part of the undercladding layer so that the entire optical mode intercepts and reflects from the mirror surface. As is well known in the field of integrated optics typically a small percentage of the optical mode power exists as an evanescent "tail" in the cladding regions. Thus, the efficiency of the mirror in reflecting mode energy is improved, somewhat, if the mirror surface extends through the upper and lower cladding layers.

#### **DESCRIPTION OF FIGS. 31-32**

10           The interconnection substrates having active layers may also be mounted vertically to a backplane (or motherboard) with optical signals being transmitted/received at the edges of the interconnect substrate, and being received/transmitted at the surface of the backplane (or motherboard). An embodiment of this configuration is shown at 200 in FIGS. 31-32, where a plurality of OE-MCM substrates 10" are mounted vertically to a  
15           backplane (motherboard) 210. MCM substrates 10" are fabricated in the same manner as MCM substrates 10 and 10' previously described, except that most of the waveguides which convey incoming and outgoing signals to the MCM substrate 10" are routed to the edge of the substrate which abuts backplane (motherboard) 210. Backplane (motherboard) 210 comprises a base substrate 212, an active layer 120", and a plurality of  
20           waveguides 224a-224g formed in active layer 120". Waveguides 224a-224g are used to convey optical signals between the MCM substrates 10". When optical switch devices (e.g., modulators) are used to transmit optical signals instead of light-emitting devices, external light power source are used. To provide external light sources, one example is to use an optical power source board 280 which interfaces to backplane (motherboard) 210  
25           in the same manner as MCM substrate 10". In this case, waveguides 224a-224g may also convey sources of light power which are provided by optical power source board 280. Power source board comprises a plurality of laser diodes LD whose outputs are routed onto waveguides of board 280, which in turn are routed to the edge of the board where it abuts to backplane (motherboard) 210. The outputs of two or more laser diodes LD may

be combined by a Y-combiner to increase the power level in such a waveguide and/or to add or multiplex light of two or more wavelengths on the same waveguide. This is shown by the middle two laser diodes LD on board 280. Multiple wavelengths of light can be separated from one another by grating filters, which are constructed in the same way as the grating beam-splitter described above. In some cases, it may be realized by forming dielectric multi-layer filters instead of metal reflective layers. Demultiplexing of the multiple-wavelength signals may be performed on the MCM or on the backplane (motherboard). Board 280 may be constructed in the same way as MCM substrates 10 and 10'.

Vertical couplers, such as coupler 160, are located within active layer 120" of backplane (motherboard) 210 to couple optical signals between waveguides 224a-224g of backplane (motherboard) 210 and the waveguides of OE-MCM substrates 10" and power source board 280. (Other optical couplers may be used, such as couplers 154 and 156 shown in FIGS. 22-23, or the same type of couplers 44 and 48 in which the mirror is formed on the end portions of the core and cladding layers). FIG. 32 shows a cross-section of the system configuration 200 in a region where the front-most OE-MCM substrate 10" abuts against backplane (motherboard) 210. For visual simplicity, FIG. 31 omitted the details of how the substrates 10" were abutted to backplane (motherboard) 210; FIG. 32 shows an example of those details. One will first see that the active layer 20" of MCM substrate 10" has been separated from the base substrate 12 along the edge where substrate 10" abuts backplane (motherboard) 210. This configuration provides several benefits. First, it enables the base substrate 12 of substrate 10" to be firmly held by a receptacle 225 without damaging the waveguides at the end of substrate 10". Second, it enables electrical traces 30' on the top surface of substrate 12 to be routed to the edge of the substrate and mechanically coupled to a conventional electrical connector 226 in receptacle 225. Thus, there is no need to form vias through substrate 12. (If substrate 12 comprises a multi-layer electrical substrate, then vias are usually present.) Each electrical signal on a connector 226 is routed to a corresponding connection pad 232 of backplane (motherboard) 210 by a respective wire 227 and connection pad 228.

Connection pads 228 and 232 are soldered together, which conveys the electrical signals, ground, and power, and which also serves to attach receptacle 225 to backplane (motherboard) 210.

As a third benefit, the separation of active layer 20" from substrate 12 enables the waveguides in layer 20" to be more accurately aligned to the vertical couplers (e.g., 160) in layer 120" of backplane (motherboard) 210. Oftentimes substrate 12 has a few microns of warpage; such warpage could cause large misalignments between the waveguides and the vertical coupler. A second receptacle 235 is adhered to the top surface of backplane (motherboard) 210, and is more accurately positioned with respect to the vertical couplers (e.g., 160) in backplane (motherboard) 210. When MCM substrate 10" is inserted into receptacle 225, the flexibility of active layer 20" enables it to be guided into second receptacle 235, and therefore into very accurate alignment in the X-axis direction with the vertical couplers (see FIG. 31 for the coordinate system definition). A standoff bridge 237 is used on MCM substrate 10" to maintain separation of layer 20" from substrate 12 in the X-direction. To achieve accurate alignment of the waveguides to the vertical coupler in the Y-direction, receptacle 235 may comprise a slot 239 (see FIG. 32) whose length is parallel to the Z-direction, and MCM substrate 10" may have a key 238 disposed on the top surface of active layer 20" and which fits snugly within slot 239. To achieve good optical coupling in the Z-direction, a small amount of optical glue or liquid refractive material may be disposed in the bottom of receptacle 235 and dried to a viscous or tacky state, and the end of active layer 20" may then contact the layer of optical glue and be adhered thereto. By directly contacting the edge of active layer 20" to layer 123, optical glue may no longer be needed to achieve substantially the same degree of good optical coupling. If necessary, anti-reflection coatings may be applied on the edges of active layer 20" and 123 to improve the optical coupling between these surfaces.

It may be appreciated that conventional optical couplers may be used to couple the waveguides from MCM substrate 10" to backplane (or motherboard) 210. This type of connection is convenient because it permits commercially available connectors to be used. In this case, two more connections per waveguide are needed, which increases the

optical loss because of the optical insertion loss of the couplers. Referring to FIG. 32, a first waveguide connector could be attached to the edge or at the surface of active layer 20" whereas a second surface normal connector could be attached to the surface of layer 123 proximate to vertical coupler 160. The first and second connector may be coupled together. However, there are optical losses associated with the transitions at each waveguides/connector interface and also at the connector/connector interface. It may also be appreciated that optical signals and optical power sources may also be provided to MCM substrates 10" by optical fibers 102, film waveguides, optical fiber array, or imaging guides, which are coupled to waveguides in the active layers 20" of substrates 10" by conventional V-groove connections 112 or surface normal connectors.

While the active layers 20" and 120" have been shown as being directly constructed on their respective substrates 12 and 212, it may be appreciated that they can be constructed separately and then bonded to respective substrates or printed circuit boards. The embodiment is shown in FIG. 32-1. This approach enables one to use different technologies for constructing the electrical interconnections and the optical interconnections. It also make it easy to separate active layer 20" from substrate 12 at the edge where MCM substrate 10" abuts to backplane 120. In the case of the FIG. 32 where active layer 20" is built up on substrate 12, a sacrificial patch of material may be disposed on substrate 12 along the edge where layer 20" is to be separated from substrate 12, and so disposed before active layer 20" is formed. After layer 20" is formed, the sacrificial patch is etched away laterally from the edge.

### **DESCRIPTION OF FIGS. 33-37**

As further inventions based on the active substrate technology, IC chips may be encapsulated in a dielectric film with contact pads formed on the film surface for attachment to an active substrate. This enables the stacking of the alternating IC chip layers and active substrate layers to form a 3-d multichip module with both electrical and optical interconnects.

FIG. 33 shows a schematic cross-sectional view of a chip layer 350 attached to an

active substrate 320. In the example shown, two chips 351 and 352 are encapsulated in a dielectric film, and the active substrate 320 comprises a VCSEL emitter device 336 and a photo-detector device 328. The chip layer 350 may be laminated to the active substrate 320 by an anisotropic conductive film 302. Such films are well known to the art. The VCSEL emitter device 336 is controlled by chip 351, and transmits an optical signal to a vertical coupler 344 in the active substrate 320. A waveguide 324a is coupled to the vertical coupler 344. Waveguide 324a conveys the signal to a transmitting vertical coupler 348, which directs the light signal to photo-detector device 328. The electrical outputs of the photo-detector device is coupled to circuitry on second chip 352. Chip layer 350 and active substrate 320 also convey electrical signals to one another through opposing contact pads 332, and may have electrical traces 330 and electrical vias 333. The contact pads 332 are coupled to one another through spheres of conductive material that is dispersed in anisotropic conductive film 302. The electrical connection provided by pads 332 is often called a Z-axis connection because the connection is made vertically, rather than in the plane of the substrate (which would be the x- and y-axes).

For the sake of visual simplicity, the structure of the active substrate has only been shown schematically with the understanding that the basic layer structure is the same as that shown in previous embodiments, and that the active substrate may be constructed with the previously described construction steps. In addition, the relative sizes of the active components to the chip and pads are not to scale. The VCSEL and photodetector (PD) are shown larger than in constructed configurations. An exemplary detailed structure of the IC chip layer and exemplary constructions steps are provided below.

Instead of joining IC chip layer 350 to active substrate 320 with a layer of anisotropic conductive material, one may use an adhesive bonding sheet. In order to join the electrical pads 332 of layer 350 to the pads 332 of substrate 320, holes are made through the bonding sheet (such as by pre-punching) in the locations of the pads, and conductive bonding material is disposed on one set of pads. Substrate 320 and layer 350 are then laminated together with heat and mild pressure. One may also use the multilayer

lamination process described in U.S. patent Application Serial No. 09/192,003, filed November 13, 1998, entitled "*Multilayer Laminated Substrates with High Density Interconnects and Methods of Making the Same*," assigned to the assignee of the present application, and invented by Messrs. Hunt Jiang, Tom Massingill, Mark McCormack, and Michael Lee. In addition, one may also use the gas-less solder paste described in U.S. patent Application Serial No. 09/203,126, filed December 1, 1998, entitled "*Conductive Composition*," assigned to the assignee of the present application, and invented by Messrs. Mark McCormack, Hunt Jiang, Solomon Beilin, Albert Chan, and Yasuhito Takahashi for the conductive bonding material used in the holes of the bonding sheet. (For diffusion bonding of two metal pads together in a Z-connection, the method newly invented by Messrs. Kuo-Chuan Liu and Michael G. Lee and described in yet to be filed patent application serial No. \_\_\_\_\_, entitled "*Transient Liquid Alloy Bonding*," (TBL) and assigned to the assignee of the present application, appears to be useful in the structures of the present application.) The Z-axis connection of pads 332 can also be done by solder joint or by metal diffusion joint. Metal diffusion joints are especially useful for making fine Z-connections (i.e., small Z-connections). In addition, the wire-interconnect structures (WITs) disclosed in U.S. patent No. 5,334,804, to Love, *et al.*, and assigned to the assignee of the present application, may also be used, preferably with an underfill material. Any of the above methods and materials may be used to join various substrates together in the previously-described embodiments, and in the embodiments still to be described below in the present disclosure. An underfill material can also be used instead of a bonding sheet for solder joints, metal diffusion joints, TLB joints, or WIT connections.

Additional IC chip layers 350 and active substrate layers 320 may be stacked upon one another and connected to one another by additional anisotropic films 302 or bonding sheets or other Z-connection methods, as shown in FIG. 34. The active substrates 320 which are within the stack are preferably separated from the base substrate 12 used to construct them, which may be done by any of the above-described substrate

separation methods. Some of the vias 333 of the layers 350 and substrate 321 may be stacked upon one another to convey ground and one or more power supply voltages to all of the layers, and to convey electrical signals from one chip layer 350 to another chip layer 350. An advantage of using a bonding sheet, or the multilayer lamination process developed by Hunt, et al., or other Z-connection methods except for those using anisotropic conductive sheets, is that optical signals may be transmitted vertically between an active substrate 320 and an IC chip layer 350 without being blocked by the conductive spheres or opaque material that is often used in anisotropic conductive films. The optical Z-connections are not shown in the figure; they can be readily realized by waveguide couplers, such as couplers 344 and 348.

The waveguides and the other active components of active substrate 320 may be fabricated in separate layers, as shown in FIGS. 35-36. In this example, the active substrate has been divided into a waveguide layer 320a and active-component layer 320b. Layers 320a and 320b are joined together by an adhesive bonding sheet 302' as described above, or by the multilayer lamination process by Hunt, *et al.*, or by solder jointing, metal diffusion bonding, TLB bonding, or WIT connection. In the case the solder joints, metal diffusion bonded joints, TLB bonded joints, or WIT connections are used, one can also use a conventional underfill in place of the bonding sheet.

FIGS. 37-1 through 37-4 shows schematic diagrams of various ways light emitter devices (*e.g.*, VCSELs) and switch devices (*e.g.*, light modulators) may be incorporated in multiple layers. In FIG. 37-1, two waveguides in two separate layers are optically coupled (optical Z-connection) to one another through a transmitting vertical coupler and a receiving vertical coupled, each of which are attached to ends of corresponding waveguides. A light modulator device is placed between in the optical path between the two vertical couplers, and is encased in a separate layer. The light modulator device comprises a body of EO material ( or electro-absorption (EA) material) and two contacts made to respective surfaces of the body. The body of EO (or EA) material may comprise an individual chip which is set during manufacturing of the layer, or the body may be formed *in situ*, such as was done for the EO material of switch device 25 shown in FIGS.



11-18. FIG. 37-3 shows the same configuration except that the bottom waveguide has been replaced by an emitter device (e.g., VCSEL). In both of these examples, the layers are built upon one another by a build-up fabrication process without the use of bonding sheets and Z-connection methods. However, if necessary or otherwise desirable, the three layers may be separately manufactured and joined together with bonding sheets, or underfill and solder joints, metal diffusion joints, TLB joints, or WIT connections. An example of this is shown in FIG. 37-2, which provides the same optical connectivity as the layer configuration in FIG. 37-3. Finally, FIG. 37-4 shows an emitter device on one layer which couples into a waveguide on a second layer without an intervening light modulator device. In the above examples, contacts to the opto-electronic devices may be routed to the bottom surface of the layer using vias. Conversely, in the examples of FIGS. 33-36, at least part of these layers can be built upon one another by a build-up fabrication process. Generally, any of the stacked structures of the present invention may be fabricated by a build-up process.

In embodiments where layers are separately manufactured and then assembled, as an option, one may use photo-refractive underfill materials or photo-refractive bonding sheets between the individual layers. With such an under fill, one is then able to form vertical waveguides through several stacked layers of components and underfill by using the SOLNET waveguide formation process described in European patent application publication No. EP-689,067-A, which is incorporated herein by reference, and which is assigned to the assignee of the present application, and which has Japanese priority patent applications JP 94-140502, JP 94-200974, JP 94-204922, JP 95-59240, and JP 95-61092. In this process, a light beam is focused on the location where the vertical waveguide is to be formed, and the photo-refractive material increases its index of refraction in response to the beam.

In FIGS. 33-37, only one light emitting device (VCSEL) and only one photo-detector device or light-modulator (switch) device have been shown for visual simplicity. Typical applications of the present invention will have several or a number of such opto-electronic devices. Instead of VCSELs, photodetectors, and optical switches, one can

use driver-integrated VCSELs, driver-integrated switches (modulators), and amplifier-integrated photodetectors, respectively. In such cases, additional pads for power supplies and ground may be needed, as previously described. Chips 351 and 352 can be VCSEL driver and/or amplifier. IC chip layers can be stacked on each other. For example a first IC chip layer for processors chips stacked upon a second IC chip layer for drivers and amplifiers, which is then stacked upon and active substrate provides a structure where outputs and inputs of the first chips layer are provided drivers and amplifiers in the second IC chip layer, which in turn coupled to OE devices in the active substrate. In this case, the connection pads of the drivers and amplifiers can be made to face the pads of the first IC chip layer. It may be possible to make vias through driver/amplifier thin film chip. Or the chip may be divided into small pieces corresponding to VCSEL and photodetectors forming vias in surrounding polymer layer. It may also be possible to use ordinary die chip (not film) for the processor. In this case a structure such as a processor die/ driver amplifier IC layer / and active substrate is constructed. In FIGS. 110 and 111 shown below, the same situation is possible. The driver/amplifier chip described above may comprise circuits such as driver circuits, amplifier circuits, bias circuits, temperature stabilizing circuits, (clock) skew compensation circuits, timing circuits, and other applicable circuits. It is also possible that chips (including driver/amplifier chips and or processor/memory chips) and OE-devices (such as VCSEL, photodetectors, and others) can co-exist in the same layer in FIGS. 33-37 and 110 and 111.

The chips in the chip layer can be thin film driver/amplifier chip with vias or divided thin film driver/amplifier chip. The structures shown in FIGS. 33-37 and 110-111 can be applied to all the embodiments described in this application, including FOLM and OE-MCM.

In addition, while non-branched waveguides have been shown in these figures for visual simplicity, typical applications will have branched waveguides, as previously illustrated in prior figures. The waveguides can be multiple-layer structures if the connection density is high. Generally, in all of the embodiments of the present application, multiple-layer waveguides may be used, as required, if the connection

density is high.

The multiple-layer structure can be fabricated by a building-up process or by a z-connection process. In some applications, the waveguide from switch devices (*e.g.*, modulators) and/or light emitting devices (*e.g.*, VCSELs) may be connected to external optical fibers, or to fiber arrays, or fiber imaging guides, or external thin films which carry a plurality of waveguides. We call the latter three external components "film waveguide arrays" or simply "waveguide arrays". These optical fibers and waveguide arrays convey light signals away from the systems created by the laminated components shown in FIGS. 33-37. In a similar manner, these external optical fibers, fiber arrays, fiber imaging guides, and waveguide arrays can convey optical signals to photo-detector devices in the active layers. In each case, the optical fiber, fiber array, fiber imaging guides or waveguide array is attached to a system layer at a place where it is optically coupled directly to an internal waveguide or to a vertical coupler or beam splitter. A waveguide array may be coupled to one of layers 320, 320a, 320b, or 350 by forming this layer to have a tab portion at one of its sides which extends past the dimensions of the laminated stack, and this attaching the external waveguide array to the extended tab. Surface normal connections can be used for the bottom and top layers. An additional benefit of this structure is that unoccupied gaps between the layers 320, 320a, 320b, 350 may also be used as channels for a coolant gas or liquid to flow through the structure.

#### **FIGURES 38-41**

An exemplary method for constructing IC chip layer 350 is illustrated in FIGS. 38-45. Referring to FIG. 38, the vias through IC chip layer 350 are first formed by taking a temporary substrate 412, and forming via posts over its top surface. Any of the previously described methods of attaching and removing temporary substrates may be used (see U.S. patent No. 5,258,236 to Arjavalasingam *et al.*). The via posts may be formed by electroplating or by sputtering, or by other methods. In the electroplating formation method, a temporary seed layer is sputtered over the surface of substrate 412, a thick photoresist layer is then formed over the substrate surface and patterned by

lithographic pattern exposure and pattern development, as is well known to the art. Via apertures are thereby formed, and conductive material is then plated into the via apertures by any conventional electroplating method. Copper material is currently preferred, but other metals may be used. One preferably plates the conductive material to a greater thickness (or height) than needed in the final structure. In a sputtering method, a thick layer of conductive material is sputtered over the entire surface of the substrate. A photoresist is then formed over the sputtered layer, and then patterned exposed and developed to leave portions of photoresist over those locations where the vias will be formed. The remaining exposed portions of the photoresist layer are then etched away.

10 After the etch, the remaining photoresist is removed.

As the next step in each of the via formation processes, the photoresist layer is removed, and the plating seed layer may be removed. As a variation to the basic method of forming IC chip layer 350, the seed layer may be retained and used in a later processing step to form the electrical traces on the bottom surface of layer 350. The seed layer may also be patterned at this general stage of the method to define the electrical traces 330 and interconnection pads 332 at the bottom surface of the IC chip layer 350. In this latter case, the seed layer is made to be relatively thick, such as by depositing additional conductive material by a blanket electroplating step. After the via posts have been formed in the photoresist layer, the photoresist layer may be pattern exposed and developed a second time (for a positive photoresist) to define the traces and pads to be formed at the bottom surface. This pattern step removes the positive photoresist in those locations where traces, pads, and vias are not to be formed. This second patterning step exposes the unwanted seed layer, which is then etched away by a suitable chemical etchant. The remaining photoresist is then removed. The definition steps of the thick seed layer may be delayed to a final step, as described below. As is well known in the art, a photoresist layer is sometimes exposed to a soft-bake step after being patterned exposed in order to improve the image. As a cautionary note, such post-exposure baking operations can reduce the amount of photo-initiator in a positive photoresist if the temperature exceeds an amount specified by the manufacturer. Thus, in order to have an

effective second exposure, the critical temperature of the photoresist should not be exceeded in any soft-bake step after the first pattern exposure. In the case that this is not possible, and also in the case that a negative photoresist have been used, one may pattern the photoresist layer by anisotropic plasma etching through an etch mask.

5 Referring to FIG. 39, the next step in the process is to attach the IC chips 351 and 352 to the surface of the temporary substrate 412. To do this, a thin polymeric adhesion layer 414 may be formed over the surface of substrate 412 by spin coating. Chips 351 and 352 (or active components) are then set in place and adhered to layer 414. Layer 414 may be soft-baked to increase its tackiness, and to reduce the amount of solvent evolution  
10 in a subsequent cure step if the material of layer 414 requires curing and contains solvent. This chip attachment step is the same step used in the previously-described method for forming active substrate 20 (FIGS. 11-18), and the reader may refer there for further details. If the seed layer in the previous step has been retained, either in whole or in patterned form, then it is preferable that a thin chromium adhesion layer be formed over  
15 the seed layer before layer 414 is formed. Such an adhesion layer is also preferred if material 414 has an unacceptably poor adhesion to the particular material of substrate 412. As another approach for attaching chips 351 and 352, a metal pad may be formed on the seed layer, and the back surfaces of the chips are coated with metal. The chips may then be attached by the previously described metal bonding and TLB methods, as  
20 well as by conventional soldering. By the time layer 350 is completed, the metal pads at the back surfaces of the chips should be electrically isolated from signal lines on the bottom surface of layer 350 (but a coupling to a fixed ground or bias potential may be used if required by the electrical circuit).

25 Since a subsequent polishing process is going to be used, chips 351 and 352 preferably have electrodes 27 which have the multilayer metal structure 27x, 27y, 27z described above (FIG. 11), with sub-layer 27y comprising a polish-stop metal like tungsten (W). This multilayer structure is best formed while the IC chips are still in wafer form (*i.e.*, not diced). If the chip has large areas of its surface in which there are no electrodes, then it is preferable to deposited an isolated patch of polish-stop material in

these areas in order to prevent dishing in the subsequent polishing process. Such a polish-stop layer is preferably formed over the chip's top passivation layer. Chips 351 and 352 may typically be manufactured with the above-described epitaxial lift-off process, which enables one to make very thin chip components (in the range of a few  
5 microns to a few tens of microns). If the chips are manufactured with thick-wafer technology, then it is preferred that the chips be pre-polished at their back surfaces to reduce their thicknesses. This may be done while the chips are still in wafer form, and such pre-polishing methods are well known to the art. Since highly uniform polishing methods are well known in the art, and continue to improve, it may also be possible to  
10 obtain thin-film chips by polishing without ELO. In this regard, a chip thickness of 5  $\mu\text{m}$  to 50  $\mu\text{m}$  is acceptable.

While FIG. 39 shows that the IC chips 351 and 352 are placed in the face up position, it may be appreciated that the chip may be placed in the face down position. If the pads and electrical traces for the bottom surface of layer 350 have been formed in the  
15 previous steps, it is then possible to not use adhesion layer 414 and to then directly contact the pads of the chips to the traces of the bottom surface by metal diffusion bonding, TLB bonding, solder bonding, WIT connection, *etc.* Once the chips have been so joined, a high-temperature underfill material may be dispensed under the chips to prevent air pockets. If the pads and electrical traces for the bottom surface of layer 350  
20 have not yet been formed, then the top surface of the IC chips 351 and 352 can be adhered to layer 414. To prevent air pockets, layer 414 may be left in a plastic flowable state at the time chips are placed and the chips may be pressed into the layer under a vacuum. Instead of this, an underfill material may be used. Placing the chips face down onto the substrate has the following advantage when using the above described epitaxial  
25 lift-off process for GaAs chips: that is the AlAs etch step (or AlGaAs etch step) used to removed the chips from the GaAs wafer may be delayed until the chips are placed faced down on temporary substrate 412. After placement on substrate 412, the AlAs (or AsGaAs) etch step is performed to separate the bulk GaAs substrate from the epitaxial layer which contains the circuits of the chip. Thus, one does not need a polymer film,

glass substrate, or other substrate to support the IC chips during the placement steps since the GaAs bulk substrate provides this function. It may be appreciated that a whole GaAs wafer may be placed face down on substrate 412, or that the GaAs substrate may be first diced to separate the individual chips from one another. In the case that the whole wafer is placed, the placement is performed before via posts 333 are formed. Another advantage of attaching the device wafer to substrate 412 is that the back surface of the device wafer can have its back surface lapped to reduce the thickness of the chips; this is especially useful for chips which are difficult or impossible to be removed by the epitaxial lift-off step.

Referring to FIG. 40, the next step in the process is to form a polymeric layer 416 over the via posts 333, chips 351 and 352, and the exposed portions of adhesion layer 414. Layer 416 will encase these components in a single polymeric film. A number of polymeric materials may be used, including core materials, cladding materials, polyimides, and photo-refractive materials. Although not necessary, photo-refractive materials should be used if one wishes to form vertical waveguides in the stacked layers with the SOLNET waveguide formation process. The polymeric layer 416 is preferably formed by spin coating the material. After the layer is formed, it is cured if the material requires curing, which is usually the case. If the thickness of chips 351 and 352 is greater than about 15  $\mu\text{m}$ , two or more separate coating and curing steps may be required for some polymeric materials, particularly those materials that undergo significant shrinkage during curing.

Referring to FIG. 41, the substrate is then polished to expose the electrodes (e.g., pads) of chips 351 and 352 and the tops of via posts 333, and to provide a more planar surface. Conventional polishing and chemical-mechanical polishing processes may be used, and such polishing techniques are well known to the art.

Referring to FIG. 42, a set of electrical traces 330 and connection pads 332 are formed over the top surface. This may be done by any conventional conductive layer formation method, many of which have been previously described and illustrated in FIGS. 11-18. For example, blanket sputtering of conductive material followed by a

patterned subtractive etch process may be used.

At this point, the processing may take different directions. If the electrical traces 330 and connections pads 332 have been previously formed by patterning a thick seed layer, as described above, then the formation of IC chip layer 350 is complete and it may be removed from the temporary substrate 412. However, before removing the temporary substrate 412, the top surface of the layer 350 may be laminated to another component layer in a Z-connection assembly step since substrate 412 can provide layer 350 with very good dimensional integrity. If the bottom traces and pads have not been formed, then the next step in the process is to attach a second temporary substrate 418 to the top surface of IC chip layer 350 using a dissolvable adhesion layer 419. Once this is done, the first temporary substrate 412 is removed. The results of these steps is shown in FIG. 43. Many dissolvable epoxy and adhesion materials are well known to the art, and are compatible with the previously-described methods for first temporary substrate 412. No further curing steps are required in the processing after this point, which significantly increases the selection of dissolvable epoxy and adhesion materials. Instead of using a dissolvable adhesion layer, one may use an ordinary adhesion layer in the substrate release technique taught in U.S. Patent No. 5,258,236, or may use a transparent substrate 418 and an adhesion layer 419 which loses it adhesion capacity when exposed to ultraviolet light. In the latter case, the substrate is released by exposing the adhesion layer to U.V. light transmitted through the transparent substrate, and then peeled off or exposed to a solvent. Other substrate release techniques described above may also be used.

Next, an optional polishing or etching step is performed to remove the polymeric adhesion layer 414, and to optionally reduce the thicknesses of chips 351 and 352. The result of this step is shown in FIG. 44.

Next, the bottom electrical traces 330 and connection pads 332 are formed, which may be done by any of the steps used for making the traces and pads at the top surface. The results of this step is shown in FIG. 45. The completed IC chip layer 350 is then usually attached to another component layer at its top surface in a Z-connection assembly



step while the temporary substrate is still in place. This provides good dimensional integrity for layer 350 in the lamination process for the Z-connection assembly. The second temporary substrate 418 may then be released from layer 350 by the appropriate removal step (e.g., such as by dissolving the adhesion layer 419 if it is dissolvable, by performing the removal steps in U.S. Patent No. 5,258,236 if that technique has been used, or by illuminating the adhesion layer 419 to U.V. light).

FIGS. 38-45 describe process steps that may be used in a variety of ways in combination with other processing steps described in the present application. For example, in addition to forming traces and pads, the bottom side processing mentioned above may also include steps for constructing other functional parts, such as 45° mirrors and optical gratings for beam splitting describe above. The process of FIGS. 38-45 may also be further modified so that the via posts are formed after the chips 351, 352 are set down. This has the advantage that the chips 351, 352 may be set down more smoothly upon the substrate. Additionally, the process steps of FIGS. 38-45 may be repeated with different device types other than chips 351, 352 (i.e., opto-electric films) and/or the device embedded on waveguide layers to fabricate a variety of single substrate or multiple substrate stacked structures.

This method of FIGS. 38-45 may be equally applied to constructing active-component layer 320b by replacing the IC chips with opto-electronic components or materials. Waveguide layer 320a may be constructed with the same steps shown in FIGS. 38-45 by adding any of the process step sequences described in this application to form a patterned waveguide core embedded in an overcladding layer and/or deleting the device-setting process. For example, via-post formation may be followed by the steps of clad-layer formation, core pattern formation, over-clad layer formation, CMP, and top metallization (or metallization prior to underclad layer formation). Waveguide layer 320a may also be formed from a subset of construction steps previously described and illustrated, such as for example, the fabrication steps of FIGS. 11-18, with the unused steps being related to the incorporation of the active components.

In all of the embodiments described in present application, and particularly those

embodiments which have fine (*i.e.*, very small) patterns and features, the polymer layers may be formed by CVD (chemical vapor deposition), evaporative polymerization, and/or MLD (molecular layer deposition) as described in U.S. Patent No. 5,444,811, which is assigned by the assignee of the present application, and/or the combination of these and other conventional coating methods. In addition, in all of the embodiments described herein, the top and bottom surfaces of the component layers may have anti-reflective layers formed on them to reduce reflection noise.

#### **DESCRIPTION OF FIGS. 46-58**

Having described several exemplary methods of forming IC chip layers 350, we provided methods of forming polymer waveguide layer 320a in addition to those described above. Referring to FIG. 46, a cladding layer 21 is formed over a temporary substrate 450 and cured in any of the above described ways. The temporary substrate 450 may comprise aluminum, quartz, glass, or any of the above temporary substrate configurations. Before forming cladding layer 21, an adhesion layer and a seed layer may be formed over the surface of substrate 450, with the seed layer being used to electroplate form via posts for conductive vias through layer 320a. Referring to FIG. 47, a core layer 24 is then formed over cladding layer 21 and cured, which may be done in any of the previously described ways. If layer 320a is to have beam splitters or wavelength filters, then core layer 24 may be etched or photo-exposed at this point to form the gratings of these components, and the gratings may then be filled with material having a different index of refraction.

Referring to FIG. 48, laser cuts are used to define the sides of the optical waveguides 454. FIGS. 48 and 49 are end views of three parallel optical waveguides.

The cladding layer 21 may be around 10  $\mu\text{m}$  thick, the core layer 24 may be around 10  $\mu\text{m}$  thick, the waveguides may be between 10  $\mu\text{m}$  to 50  $\mu\text{m}$  wide, and the waveguides may be spaced apart from one another by a pitch of around 250  $\mu\text{m}$ . The laser cuts need only be as deep as the core layer 24, but in practice sometimes are as deep as the combined thickness of the cladding and core layers 21, 24. The width of the laser cuts

may be around 20  $\mu\text{m}$  to 75  $\mu\text{m}$ . A cleaning operation is preferably performed to remove debris from the laser cutting step. This clean may be performed by a plasma etching step, which tends to etch debris at a faster rate than cladding and core layers 21 and 24. To reduce the amount of debris that needs to be removed, one may form a layer of

5 photoresist, or other uncured polymeric material, over the core layer 24 before the laser cutting operation is performed. During the cutting operation, a major portion of the debris will be left on top of the photoresist layer, and may then be easily removed by removing the photoresist layer by exposure to a solvent or developer solution. A brief plasma etch may then be done to ensure that the laser etched trenches are clean.

10 Referring to FIG. 49, a top cladding layer 23 is formed over the patterned core layer 24 and then cured by any of the previously described ways of forming cladding layers. At this point, via posts may be formed by laser drilling apertures to the seed layer, cleaning, and then plating. Also, the electric traces and pads at the top surface of cladding layer 23 may be made.

15 Referring to FIG. 50, which shows a side view of the parallel waveguides, laser cuts, such as those formed by laser ablation, are made at the ends of the waveguides to form the bevel edges for the mirror elements of the vertical couplers. The angle of these cuts may be inward, as is shown in view A at 455, or they may be outward, as is shown in view B at 456. A waveguide may also have an inward cut at one end, and an outward cut

20 at the other end. If necessary, patches of metal may be formed at each laser cut site in order to provide more accurate laser cuts, as previously described above (see FIG. 27, layer 161). After this step, the beveled edges may be cleaned by a brief plasma etch step, and a layer 458 of reflective metal or reflective material is deposited over the beveled edges left by the outward laser cuts 456. If electrical traces and pads have been previously

25 formed on the top surface of cladding layer 23, and if one forms the mirrors with a blanket deposition of reflective metal, then it is preferable that one first forms a photoresist lift-off layer over these traces and pads before the laser cut operation and the blanket deposition steps are preformed.

To form the mirror elements on the bevels of the inward cuts, a second temporary

substrate 452 is attached to the top of layer 320a by any of the previously described methods, and the first temporary substrate 450 is removed, as shown in FIG. 51. In the embodiment shown in FIG. 51-1, an adhesive layer 453 is shown between second temporary substrate 452 and layer 320a. The bevels are cleaned with a brief plasma etch, and then coated with a layer 457 of reflective metal or a reflective material. Electrical traces and pads may then be formed on the bottom surface of layer 320a. Layer 320a is thus completed, and may then be assembled to an IC chip layer 350 or an active component layer 320b, after which the second temporary substrate 452 may be removed. As another approach to forming the mirror elements on the bevels of the inward cuts, one may deposit reflective metal on the inner surface by direct electroplating, electroless plating, direct plating, or high-pressure CVD (10 milli-torr to 100 milli-torr) before the second temporary substrate is attached. In the case of direct electroplating, the seed layer must be present. In the case of electroless plating, one exposes the surfaces of the polymeric material to appropriate activation and catalytic treatments.

In a modification of the process shown by FIGS. 46-51, the waveguide are defined by plasma etching of core layer 24 rather than by laser cutting. After the core layer has been formed and cured (FIG. 47), an adhesion layer, such as one comprising chromium, is formed over layer 24. A thick photoresist layer is formed over the adhesion layer and then patterned to define the locations where the waveguides 454 are to be formed. The exposed portions of the chromium adhesion layer are etched away by a quick chemical etchant for chromium, and the resulting structure is plasma etched to remove the exposed portions of layer 24, as shown in FIG. 52. A little over etching into bottom cladding layer 21 is preferably performed to ensure that no waveguide will have any leakage of light. After the plasma etch, the remaining photoresist and adhesion layers are removed, and cladding layer 23 is formed and cured (FIG. 53). The remaining processing steps illustrated by FIGS. 50 and 51 are then performed.

As previously discussed, in an alternate process, the core may comprise a photo-sensitive material, which is hardened by light exposure. For this case, the core patterning may be done by a patterned exposure process instead of by a RIE process. In this case,

in addition to laser cutting or a RIE technique, a tilted lithographic exposure technique, such as that disclosed in Japanese Patent Application JP 96262265, can be used for making beveled edges. Direct exposure through a photomask is preferable for process simplicity. However, if the surface is stable enough after soft curing, a metal mask may be formed on the surface to act as photomask. If further planarization is desired, CMP can be applied after the over cladding layer is formed.

Generally, it is simpler to fabricate the outward cut mirror of FIG. 50-2 rather than the inward cut mirror of FIG. 50-1, although it is desirable to be able to economically fabricate both types of mirror structures. Referring again to FIGS. 50-1 and 50-2, inward cut and outward cut mirrors both define trapezoidal shapes that are the mirror images of each other. If the top surface of the trapezoidal surface of FIG. 50-2 is attached to an OE substrate, it will perform as an inward cut mirror on the OE substrate to which it is attached. Consequently, a mirror fabricated as an outward cut mirror, as shown in FIG. 50-2, may be attached to another OE surface so that it functions as the inward cut mirror of FIG. 51-2. This method facilitates a high-yield process for fabricating a multiple-layer OE substrate having inward cut mirrors.

FIGS. 54-58 illustrate an exemplary method of adding an active component layer to the waveguide layer. The waveguide layer and via posts of FIGS. 54-58 may be formed by the previous methods, such as the methods illustrated with FIGS. 38-45 and FIGS. 46-53. Starting with the waveguide layer 320a shown in FIG. 51, the voids created by cuts 455 and 456 are filled with material (usually polymeric material), and the surface is planarized. electrical traces and interconnection pads are formed over the exposed surface of cladding layer 21, and via posts are formed by electroplating by via formation steps previously described. The result of these steps is shown in FIG. 54. Next, referring to FIG. 55, a VCSEL emitting device 36 is placed face down on the substrate, and has its electrodes joined by metal-diffusion bonding to corresponding pads 332 and/or traces 330 that are formed over cladding layer 21. A high temperature underfill is then preferably dispensed under the emitting device 36. Other devices, such as photo-detecting devices, are similarly attached and processed, but are not shown in the figures for visual

simplicity. Each of the devices so placed in FIG. 55 have the active area overlying a mirror structure 458 at an end of a waveguide, or at a branch of a vertical beam splitter.

Referring to FIG. 56, a polymeric layer 25 is then formed over the surface to encase device 36 and vias 333 in film of polymer material. Any type of material may be used, including cladding material, core material, polyimides, and photo-refractive material (which would be useful for making vertical waveguides by the SOLNET process). Layer 25 is cured, if needed, and then polished to expose the tops of vias 333, to make layer 25 more planar, and to optionally expose the surfaces of the devices embedded in layer 25, if such is necessary (such as to make additional electrical contacts to the components). The result of these steps are shown in FIG. 57. Next, as shown in FIG. 58, electrical traces and pads are formed on the top surface of polished layer 25. The traces may be formed by any of the previously described pad/trace formation steps. An active substrate 320 is thereby formed, which may be assembled to an IC chip layer 350 (or any other active layer, including waveguide layer, or chip) using temporary substrate 452 for dimensional control. The assembly may be done by any of the previously described methods. After assembly, temporary substrate 452 may be removed by any of the previously described substrate-release methods.

Alternately, it may also be possible to stack waveguide layers on the active device layer in a similar manner to that shown in FIGS. 54-58. For this case, the VCSEL should be placed in a face-up position. Additionally, various combinations of layers, such as waveguide layers, active devices layers, chip layers can be build-up using any combination of steps shown in FIGS. 38-58.

#### **DESCRIPTION OF FIGS. 59-68**

As indicated above, when one uses switch devices or lateral light-emitting devices which are pre-built on chips which have high indices of refraction compared with the index of the waveguide material, in some cases it is advisable to narrow the width of the device with respect to the width of the waveguide in order to provide good optical coupling between the waveguide and the chip device. A high coupling coefficient

between a waveguide and chip device is desirable because it increases the efficiency of a variety of electro-optic processes. For example, a high coupling coefficient permits lower voltage switches and modulators to be used, because the optical mode interacts strongly with the switch/modulator. Narrow device widths of the active devices enables higher speed operation by decreasing device capacitance. By the same reasoning, it is also advisable to reduce the height of the chip component with respect to height of the waveguide, and to center the chip in the middle of the waveguide. Decreasing the thickness of the active devices enables lower power (voltage) operation by increasing the electric fields in the devices. Steps for performing the centering of chips with reduced height are described below, and these steps may be incorporated into the construction methods previously described. FIGS. 67 and 68 show the result that is desirable to obtain, where FIG. 67 is a top plan view and FIG. 68 is a cross-sectional view. Four switch devices 26a-26d in chip form, and having a high index of refraction, are coupled in line with four respective waveguides 24a-24d having greater widths and thicknesses. To reduce reflects at the interface between the waveguides 24a-24d and the devices 26a-26d, the ends of the devices 26a-26d are tapered. The amount of tapering, and the amount of width reduction between each device 26 and its waveguide 24, for optimal coupling is dependent upon the difference in indices of refraction. The values needed for optimal coupling are best computed through optical simulations. FIG. 68 is a cross-sectional view showing how the chip of switch device 26b has a lower height than the height of waveguide 24b, and how the chip is centered in the middle of the waveguide. The centering is achieved by a pedestal of cladding material 21b, which in turn is formed on a bottom cladding layer 21a.

Referring to back FIG. 59, we now describe exemplary steps for constructing the structure shown in FIGS. 67-68. Starting with a base substrate 12, a first cladding layer 21a is formed over the surface of base substrate 12, and cured. Cladding layer 21a may comprise any of the cladding materials previously described. Next, a second cladding 21b is formed over cladding layer 21a. This cladding layer can be any of the previously described cladding materials, including photosensitive cladding materials. Before

cladding layer 21b is cured, a device chip 26 is adhered to it, such as was done in the previous construction methods. Layer 21b is then soft-baked to remove the solvent used to fluidize the polymeric cladding material. The results of these steps are shown in FIG. 60, which shows a cross-sectional view, and in FIG. 61, which shows a top plan view. If cladding layer 21b is not a photosensitive material, it is preferably cured at this point. (During these steps, appropriate electrode structures may be formed in the layers, as describe above; these steps are omitted here for the sake of brevity, but it will be apparent to one of ordinary skill in the art how these steps are incorporated given the previously-described construction methods).

At this stage of the process, chip 26 is a large piece of material which is now patterned to define the individual devices 26a-26d. This may be done by forming a photoresist layer over the top of cladding layer 21b and chip 26, pattern exposing and developing the photoresist layer it to leave patches of the photoresist over chip 26 where the individual devices 26a-26d are to be formed. The exposed portions of chip 26 are then etched away by a suitable etchant to define the individual devices. The results of these steps are shown in a cross-sectional view of FIG. 62 and in a top plan view of FIG. 63. This patterning and etching step also provides the tapers of the chip devices. If chip 26 is a multilayer structure, several etch exposure steps, using different etchants, may be needed.

If cladding layer 21b comprises a photosensitive material, then the pattern exposure of the photoresist layer could also pattern all of the portions of cladding layer 21b which are not under the whole chip 26, if a sufficiently long exposure is used. In this case, portions of cladding layer 21b would be removed in the development step of the photoresist layer. However, this is of no detrimental consequence. If one wishes, one can adjust the energy of the exposure step such that the photoresist layer is fully exposed but the cladding layer 21b is not fully exposed. One may also use portable conformal masking structures to avoid exposure of cladding layer 21b at this point.

As the next step, all portions of cladding layer 21b which are not underneath the patterned devices 26a-26b are removed. If layer 21b is photosensitive, this may be



accomplished by performing a blanket exposure to actinic radiation, using the individual chips 26a-26d to block the radiation from hitting the locations where cladding layer 21b is to be retained. The cladding layer 21b may then be developed and then cured. This provides a self-aligned patterning of layer 21b, and the results of these steps are shown in the cross-sectional view of FIG. 64. Any photoresist material left on top of the individual chips 26a -26d in the previous patterning step will be exposed in this blanket exposure, and thus can be removed by a developer solution, sometimes by the developer used in the development step for cladding layer 21b. If the photoresist layer and the cladding layer 21 have incompatible chemistry, or if the solvent of the photoresist would dissolve cladding layer 21, then a barrier layer may be formed between these two layers. The layer is preferably opaque, and is removed after the photoresist layer has been used to pattern the devices 26a-26d. Cladding layer 21b may then be defined by a blanket exposure, as before. A chromium or tungsten layer may be used as the barrier layer.

If cladding layer 21b does not comprise a photosensitive material, the unwanted portions of cladding layer 21b may be removed by plasma etching, using the individual chip as an etch mask, along with the photoresist patch above it, if so desired. In this case, any excess photoresist may be stripped away after the etch step. While the etch time can be controlled to only etch layer 21b, one can form a plasma-etch stop layer over layer 21a before layer 21b is formed, and can remove the plasma-etch stop layer after layer 21b has been defined by the plasma etch step. A chromium layer may be used for this purpose.

The next step in the process is to form a core layer 24 over the resulting structure, as is shown in FIG. 65. The core material is then patterned to define the waveguides, as is shown in the top plan view of FIG. 67 and the cross-sectional view of FIG. 66. Any of the previously described patterning methods, including the use of a photosensitive or photo-refractive material and photo-exposure, may be used. The ends of the waveguides preferably abut the taper sides of devices 26a-26d, or penetrated part way into the taper sides. As the next step, a layer of cladding material 23 is formed over the structure and cured, as shown in FIG. 68. Additional processing steps to form traces, pads, mirror elements, beam-splitter elements, and other features previously described may be

undertaken at this point.

When metal electrodes are formed on or in the second cladding layer 21b, mini chips can be placed on these metal electrodes and coupled thereto by the previously described metal diffusion, metal bonding techniques, TLB, and solder bonding.

5 Additionally, if metal electrodes are formed on the top surface of a mini chip, one or more of the chip's electrodes may be bonded to metal pads formed on the top surface of cladding layer 23. This provides both electrical connection and physical attachment. Additionally, if a signal to the mini chip comes from a trace on the opposite surface, the via between surfaces may be located under the connection pad to provide for a more compact connection arrangement. This provides for efficient use of surface area for making the electrical connections to the mini chips.

10 In the core layer coating step shown in FIG. 65, an optional clad layer can be coated on the core layer. After the core layer is cured, the optional cladding layer is coated followed by soft and full curing. If the core layer thickness is a little bit thinner than OE device height, the polished surface can be in the cladding layer. This two-layer approach may improve the interface flatness between core and clad layer, thereby reducing optical scattering losses. Alternately, optical scattering losses may be reduced if the CMP process is applied after the over cladding layer formation.

15 In some process variations, one or more CMP steps may be eliminated to reduce the optical scattering losses associated with the optical mode scattering from the CMP planarization surface. When a photo-sensitive waveguide material is used, such as one that is hardened by light exposure, CMP planarization proximate to the core layer is not necessary. After the step shown in FIG. 65, waveguide patterning can be carried out by patterned light exposure. A planarization step may be applied after the overladding layer is formed, if necessary.

20 As another variation on the core patterning process, the minichips may include core and cladding structures prior to attachment of the minichip to the cladding layer 21b in FIG. 60. For this case 26, 26a, 26b, and 26c are replaced by elements 26', 26a', 26b', and 26c' as shown in FIGS 60-2, 61-2, and 63-2. This has several advantages.

The refractive index profile can be controlled towards the edges of the mini-chip. In particular, the refractive index of the chip core and chip cladding can be very close to each other (small refractive index step) which facilitates increasing the beam spot size at both edges of the minichip for efficient optical coupling to waveguides.

5           The embodiments shown in FIGS. 11-20, 59-68, 74-81, and 82-89 are exemplary. One of ordinary skill in the art may combine aspects of one or more of these and other embodiments herein together according to the requirements of a particular application.

10           The method shown in FIGS. 59-68 may be utilized with a variety of non-epitaxial films as well. For example a large refractive index films, such as a  $\text{TiO}_2$ ,  $\text{WO}_3$ ,  $\text{SiN}_x$ , or Si film can be embedded in the same ways. These films can be obtained as an lifted-off film using a substrate that can be selectively removed, such as a Si, metals, or polymer substrate. A high refractive index waveguide may be used as an optical delay line. If a rare-metal-doped glass film is embedded, then it may be used as an optical amplifier. Other optical films, such as luminescent films, photo-refractive films , and nonlinear  
15           optical films may similarly be incorporated as optical waveguides using the method shown in FIGS. 59-68. When the refractive index of the embedded film is larger than the core material, the core materials can be used for layer 21b. In this case, the etching of the core layer on the embedded film (FIG. 66) is not necessary and the overclad layer can be coated after the step shown in FIG. 65.

20           The previously described fabrication processes may also be used to fabricated films with active OE devices but no waveguide layer. FIGS. 147-153 show an exemplary process to fabricate an OE film with embedded devices. Electrical pads, electrical lines, and electrodes are formed on a substrate (FIG. 147). Thin film devices are then placed on the metal pads/lines on the substrate (FIG. 148). The thin film devices may be any thin  
25           film device such as those fabricated with an ELO process. A polymer film is then used to coat the substrate, embedding the thin film devices in the polymer (FIG. 149). The polymer is then planarized to the level of the thin film devices by polishing (FIG. 150). Surface contact pads and vias are then formed on the planarized polymer (FIG. 152). The substrate of the OE film may then be removed, either before (FIG. 152) or after

(FIG. 153) the OE device film is attached to another layer, such as a waveguide layer. Alternately, via posts may be fabricated after the thin film device placement step, followed by the embedding, planarization, and contact pad formation steps. Still yet another option is to insert a buffer polymer layer between the substrate and pads, electrical lines, and electrodes, regardless of how the vias are formed.

#### **DESCRIPTION OF FIGS. 69-72**

Additional multichip module interconnection configurations are now described. These modules may be constructed by the above described construction methods. A free-space optical interconnection system is shown in FIG. 69 where optical signals are conveyed through free space between two laminated boards 501 and 502. Each laminated board 501-502 has a plurality of optical switches 506 which transmit light to opposing photo-detectors 508 through a section of air, or free space. Each optical switch is feed with optical power by a waveguide 503, which may have grating beam-splitters 504 to convey the power vertically to one surface of the switch 506. The light enters perpendicular to the surface of the optical device (e.g., a mini-chip of EA or EO material), and exits perpendicular to the opposite surface of the optical device. Before the light exits each board 501 and 502, it passes through a micro-lens 511 formed in a material layer 510. The light also passes through another such micro-lens before it enters a photo-detector device 508. The micro-lens is a section of material which has a higher index of refracting than the bulk material of layer 510, and it serves to focus the light as it is emitted and as it is collected. While the micro-lens may be used by itself, other optical elements may also be inserted between boards 501, 502 to adjust the optical focus of the micro-lens, if required.

The micro-lens is preferably made by the SOLNET process by using a sheet of phot-refractive material (e.g., polyguide from DuPont), and exposing it by writing beams to form the micro-lenses. The cross section of each micro-lens, as looking from the top surface of layer 510, is circular or square. The surfaces of layers 510 may be coated with anti-reflective materials to improve optical coupling. In addition, optical materials

having an index of refraction close to that of the micro-lenses may be disposed between boards 501 and 502 to improve optical coupling.

The layer of boards 501 and 502 have been separately constructed and then laminated together, according to the processes above. Between each layer, a bonding sheet or underfill may be used to improve optical coupling between the devices and the micro-lenses, and between the power waveguide 503 and the optical switches 506. These layers, of course, may be integrally formed, which is shown in FIG. 70 by boards 501 and 502.

The primary difference between the embodiment of FIGS. 69-70 and that of FIGS 35-37 is the use of vertical optical switches (or light modulators) instead of VCSELs for the transmitters. However, micro-lens array may be used in conjunction with any of the techniques to couple light to the optical switches 506 mentioned in this application. For example, instead of using a grating for coupling optical power supply to a switches 506, forty-five degree mirrors could be used. Alternately, branched waveguides in the manner of FIG. 37 could be used to coupled light to optical switches 506. The vertical optical switches 506 may also include a variety of switch structures, such as EA modulators.

This concept may be extended to form vertical optical connections in stacks of active layers 320 and IC chip layers 350, as is schematically illustrated in FIG. 71. In FIG. 71, active components, such as VCSELs, photodetectors, and modulators are omitted for the sake of clarity, but may be included in a substrate with vertical couplers. As shown in FIG. 71, the layers are made from a photo-refractive material. The SOLNET process may be used to fabricate the vertical micro-lenses which, when stacked upon one another, form a vertical waveguide, or so called optical Z-connection. Bonding sheets made of photorefractive material may be used to laminate the active layers 320b, waveguide layers 320b, and IC chip layers 350 together. For the fabrication of the optical z-connection in each layer, other methods can be applied in addition to SOLNET.

The vertical optical connections may be organized in separate units 710 which are coupled to two sides of a set of active substrates 705, as is shown in FIG. 72. The active

substrate 705 may take the form shown in FIG. 35. Units 710 have a plurality of vertical waveguides formed through their Z direction, and which optically connect to waveguides at the edges of substrates 705. Units 710 may be constructed using the sequence of fabrication steps shown in FIG. 73. Staring with a plurality of sheets of refractive material (e.g., polyguide), short sections of bonding sheets are attached to the left edges of the sheets. The sheets are then bonded together, and then the SOLNET process is applied to the right edges of the photo-refractive sheets (use of writing beams) to form the vertical waveguides. The sheets are then cured, and are then assembled to the substrates 705.

FIGS. 109-111 show alternate OE-3D stack configurations. Chips may be embedded in a variety of different OE-film substrate structures comprising active and passive device films to form optical interconnections.

FIG. 112 shows how in the present invention a plurality of OE films may be stacked using an optical Z-connection to construct multiple-layer OE substrates. As shown in FIGS. 113-116, a stacked may comprised a variety of different film types. As shown in FIG. 113, the OE film may comprise a passive polymer waveguide, with additional electrical lines, pads, vias, electrical voltage planes, and ground planes. As shown in FIG. 114, the polymer film may comprise OE devices embedded in the polymer film with additional metalization. The active OE devices may include any of the previously mentioned devices, such as VCSEL, light modulators, optical switches, optical amplifiers, wavelength filter, tunable filter, wavelength converter, photodetectors, driver chips, amplifier chips, LSI, optical components, and resistors, capacitors, and other electrical components. Mini-chips, in which a plurality of components are integrated, can also be embedded. In the embodiment shown in FIG. 115, both passive waveguides and active OE devices may be integrated into one film, along with additional via and contact metallization. FIG 115 shows a first embodiment having both waveguides, VCSELs, and photodetectors whereas FIG. 116 shows light modulators and photodetectors coupled to waveguides. More complex multi-layer waveguides may also be included in the embodiments of FIGS. 113, 115, and 116.

The ability to stack different OE film types using electrical and optical Z connections permits a variety of package structures. FIGS 117-120 show side views of film optical link modules (FOLM). The FOLM structure permits optical signals to be conveniently extracted from a chip, CSP, or MCM to be linked to other boards and/or other system elements, giving the system engineer the flexibility to optically link modules of chips in a wide variety of ways. As indicated in FIG. 117, an OE film (OE-film-DW) with waveguides, VCSELs and photodetectors may be used for E/O and O/E conversion. VCSEL with an integrated driver, and a photodetector with an integrated amplifier may also be used. A fiber array, image guide, or waveguide array is connected with a connector to the waveguides at the edge of the OE film, thus forming an optical link to other elements. The VCSELs, in response to outputs of a chip, emit optical signals which are transmitted through the optical link (fiber array, waveguide array, or image array) to a board or unit which is connected to the OE-film. The fiber array, image guide, or waveguide array is preferably connected to other boards or units to enable an optical interconnections between boards and/or units. Conversely, optical signals coupled to the waveguides via the optical link from outside of the OE-film are received by the photodetectors in the OE-film. The optical signals are converted into electrical signals, which are input to the chip.

As shown in FIG. 118, the same function may also be achieved by stacking a passive waveguide substrate (OE-film-W) with another substrate having only active OE devices (OE-film-D), in the manner of an interposer. The VCSEL performs an E/O conversion function in response to the chip output whereas a photodetector performs an O/E conversion function in response to an received optical signal. FIG. 119 shows a FOLM embodiment in which an OE substrate with waveguides, VCSELs and photodetectors (OE-film-DW) under a MCM upon which chips are mounted. FIG. 120, shows a FOLM embodiment similar to FIG. 119 except with a passive waveguide film (OE-film-W) and active OE device film (OE-film-D).

The structure of FIG. 119, the OE film is stacked on the substrate without its left edge extending beyond the edge of the substrate. The horizontal optical connector used

in FIGS. 117-118 is replaced by a vertical two-dimensional optical connector to the OE film. This vertical connector couples the waveguides in the OE film to the end of a two-dimensional (2D) fiber array (or fiber image guide). In location of the vertical connector, vertical couples (e.g., mirrors) are formed in the OE film to turn the optical signals in the  
5 OE film towards the 2D fiber array. In turn, the ends of several waveguide cores in the 2D fiber array terminate at the connecting face of the vertical connector, with each waveguide end being positioned over a corresponding vertical connector in the OE film. This type of surface normal coupling is effective for massive parallel interconnections, and is preferred for such types of applications. This surface normal coupling may be used  
10 with any of the embodiments of the present application where an OE film is optically coupled to (2D fiber arrays (or fiber image guides).

As we previously stated, the stacked structures shown in FIGS. 33-37 and 110-111 may be used in constructing FOLM structures. For example, in FIGS. 117 and 119, the driver/amplifier chip layer can be stacked on an OE-Film-DW to act as a interface  
15 between OE devices (e.g., VCSEL, photodiode, modulators, etc.) and the input/output terminals of chips or MCM modules. For FIGS. 118 and 120, the driver/amplifier chip layer can be stacked on an OE-Film-D. In both cases, OE-film and driver/amplifier chip layer can be stacked by a Z-connection (lamination) process or by a build-up process. Of course, the driver/amplifier chip layer may include any auxiliary circuits, such for  
20 example driver circuits, amplifier circuits, bias circuits, temperature stabilizing circuits, skew compensation circuits, timing circuits, and other appropriate circuits. It is also possible that the chips and OE devices may co-exist in the same layer (OE-film).

In comparison, the distances between electrical input/output terminals, and between E/O and O/E conversion parts are smaller those distances in conventional optical  
25 link modules. This improves interconnection performance. Furthermore, in conventional optical link modules, extra space is needed. Small or no extra space is needed in the FOLM structures of the present application.

FIG. 121 is a top view of a FOLM structure in which a portion of the OE film preferably has sufficient room so that the waveguides may be curved in order to adjust, if



required, the optical path lengths to mitigate signal skew. More generally, it is desirable to adjust the waveguide routes, or path lengths, so that signals have the same transit time from the output to the input of various chips/regions, boards, units, or modules. Other techniques to adjust transit time, such as varying other waveguide parameters (e.g., refractive index) may also be utilized so prevent skew.

As shown in FIGS. 122 (top view) and 123 (side view), the connector preferably includes a connector buffer to perform optical adjustment functions which facilitate communicating signals to a connector. For example, a connector buffer may adjust spot size, and change the waveguide pitch (i.e., waveguide separation). For example, the connector buffer may have curved waveguide paths so that one or more planar, one-dimensional arrays of polymer waveguides are coupled to a two-dimensional array of waveguides. As indicated in FIG. 121, an extended portion of a flexible substrate region may be patterned into ribbons, each containing a plurality of waveguides. A plurality of ribbons may each be twisted so that the end of the ribbons forms a two-dimensional waveguide array. For a ribbon length of five centimeters, an individual ribbon may be twisted by ninety degrees with relatively low stress. A polymer film thickness in the range of about 10-to-250 microns is preferred. Each ribbon may, for example, contain 12 waveguides with a pitch in the range of about 30-to-250 microns. The edges of a plurality of ribbon may then be stacked into a frame-connector and polished to form a 2-D waveguide connector. The outer surface of the connector buffer is also preferably shaped (e.g., polished, sliced, or otherwise shaped to form a coupling surface with a planar surface) to facilitate coupling to external optical connectors. This permits the waveguides of the FOLM to be coupled to a variety of optical couplers, such as two-dimensional fiber arrays and image guides. FIG. 124 shows how optical signals in the connector buffer may be routed to a two dimensional waveguide array connector comprising a plurality of waveguide cores arranged in an array. The connector buffer preferably performs an optical adjustment function so that a plurality of waveguides of an OE film are optically coupled to a commercially available optical connector, such as a two dimensional optical connector. The MT connector, available from Furukawa

Electric, Co., Ltd, Tokyo, Japan, is an example of a preferred multi-fiber connector. The connector buffer can also include wavelength-division multiplexing (WDM) functions, such as wavelength multiplexers (MUXs) and wavelength demultiplexers (DEMUXs), etc. to add WDM capability to the FOLM structures according to the present invention.

- 5 In the case of surface normal 2D connectors shown in FIG. 119, the same functions and components described above may be used.

FIG. 125 shows a high speed FOLM embodiment. High speed optical modulators are driven by the outputs of a chip to generate optical signals from externally input light. The light modulator can operate with low current and low power dissipation compared with VCSELs. A high-speed and low heat-generation opto-electronic amplifier/driver-less substrate (OE-ADLES) is preferably used at high optical signal levels. In OE-ADLES, the light modulator may be directly driven by chip outputs because it has voltage-drive characteristics that are compatible with the outputs of a chip. Consequently, an additional driver is not necessary to drive a modulator from a chip.

10 Additionally, by increasing the input optical power, the optical signal at the photodetector is sufficiently strong so that a photodetector amplifier may be eliminated. An OE-ADLES apparatus and method is described in the paper of Yoshimura, *et al.*, "Optoelectronic Amplifier/Driver-Less Substrate ,OE-ADLES. For Polymer-Waveguide-Based Board Level Interconnection-Calculation Of Delay And Power Dissipation,"

15 submitted at the 8<sup>th</sup> Iketani Conference, 4<sup>th</sup> International Conference On Organic Nonlinear Optics (ICONO'4), October 12-15, 1998, Chitose, Japan, the teachings of which are hereby incorporated by reference. OE-ADLES is preferred because it permits the elimination of drivers and amplifiers that increase the cost and complexity of the OE substrate as well as decreasing signal delays due to drivers and amplifiers.

25 A FOLM may comprise a variety of OE film substrate stacked structures. FIGS. 126-129 show details of preferred embodiments of a FOLM structure. FIG. 126 shows a side view of a FOLM structure. FIG. 127 shows a top view of the entire FOLM structure with spot size converters to couple the FOLM waveguides to commercially available MT connectors. As can be seen in FIG. 127, each of 16 MT connector outputs 12 waveguides

of the FOLM, so that there are 196 channels for the communication of optical signals in the FOLM. Since the core of a commercially available MT connector has a core that is 62.5 microns x 62.5 microns, a 5 centimeter length of the FOLM serves as a connector buffer to gradually increase the spot size of the OE waveguides (core dimensions of fifteen microns by fifteen microns) and translate the waveguides to efficiently couple to the MT connector.

FIGS. 128 and 129 show a detailed view of a portion of FOLM structure illustrating how the preferred fabrication method results in VCSELs that are electrically and optically coupled to waveguides by metallized forty-five degree mirrors. As can be seen in FIGS. 128 and 129, a portion of the Au contact layer of the VCSEL is electrically connected to the mirror metalization, facilitating a convenient electrical connection to the VCSEL. The optical emitting window of the VCSEL, which has an area on the order of about ten microns by ten microns, is orientated so that it impinges upon the metallized mirror and is reflected into the waveguide.

An exemplary fabrication process for a FOLM structure includes the steps of forming a first polyimide film, preferably on an Aluminum substrate, glass, quartz, or other suitable substrate which can later be preferentially removed. After the first polymer layer is formed, contact pads and electrodes are deposited on the surface of the polymer layer. The pads are patterned for mounting VCSELs. ELO VCSELs and photodetectors are placed onto the contact pad. Preferably a Au/Sn/Au metal diffusion is used to bond the VCSEL to the contact pad. A second polyimide layer or other suitable polymer layer is then coated over the VCSELs. The surface is then planarized with CMP. A waveguide clad fluorinated polyimide layer is then formed over the planarized wafer. A core layer is then deposited, patterned, and embedded in an over-clad coating in the manner described in regards to previous embodiments. Forty-five degree mirrors are formed in any of the previously described fabrication processes, such as by RIE and laser ablation. The mirror surfaces are then metalized. The same metalization is preferably used to contact the electrodes of the VCSELs and/or pads and/or vias for the VCSELs. A polyimide layer is coated over the substrate and planarized by CMP, if necessary. The Al

substrate is then removed and the first polyimide layer is removed or etched to make electrical contacts and/or pads and vias to the OE film. Alternately, removal of the Al substrate can be performed after the OE film is attached to another substrate.

As shown in FIGS. 130-137, a plurality of chips/CSP/MCM can be mounted and electrically and optically coupled using an opto-electronic interposer (OE-IP) or OE-film MCM fabricated from the previously described fabrication processes. An OE-IP is inserted between a chip, CSP or MCM and a single or multiple OE layers, and preferably provides an optical connection to at least one other element. Multiple OE layers can also be built up by the same method described earlier. The OE layers can be stacked by solder bonding, TLB, WIT, metal diffusion, and the method disclosed in U.S. patent No. 5,334,804, conducting paste or other building-up processes. One preferred paste lamination is the MAJIC paste lamination process, which is disclosed in MAJIC paste lamination, which is disclosed in U.S. Patent Application Serial No. 09/192,003, and which is assigned to the Assignee of the present invention, the teachings of which are hereby incorporated by reference.

The OE-IP of the present invention may comprise a variety of light sources and/or photodetectors or other components and/or integrated components disposed in the OE-IP in a variety of ways. In the embodiment of an OE-IP of FIG. 130, VCSEL and photodetectors are embedded in the polymer film of the OE-IP. FIG. 133 shows an OE-IP using light modulators coupled to a light source instead of VCSELs the optical transmitters. The light source may be supplied from light sources on the OE layer or OE-IP. The light source may also be supplied from an external source via an optical fiber, optical fiber array, imaging guide, or flex waveguide array, as shown in FIG. 134. Suitable light modulators include electro-optic devices such as Mach-Zehnder modulators, internal total reflection switches, digital switches, directional coupler switches, or electro-absorption (EA) modulators.

FIG. 138 shows a case that OE-IP optical interconnections are on the opposite side of the chip/CSP/MCM-mounted surface compared to FIGS. 130 and 131. The VCSELs and photodiodes are embedded into the OE layer near the bottom surface.

FIG. 135 shows an example of an OE-IP with optical interconnections to chips/MCMs mounted to both sides of the OE-IP. The OE-IPs can be merged in OE layer. This means VCSELs and photodiodes are embedded into the OE layer near the bottom and top surfaces.

5           The OE-IP of the present invention may also be used in a variety of ways with other OE layers. FIG. 139 and FIG. 130 are examples of OE-IP. FIG. 131 and FIG. 140 illustrate OE-film-MCM. FIGS. 136-137 show an OE-IP with external or flexible interconnections. The flexible interconnection enables the OE-film-MCM to be used as a parallel optical link module. As shown in FIGS. 136-137, the flexible optical connector  
10       can be attached at least to the edge of the OE-film-MCM. The flexible interconnection is useful for a variety of purposes, such as coupling a source of light power for optical signals and to provide a means of coupling to another OE-IP or OE layer. However, a flexible interconnection is also useful for forming a film optical link module (FOLM) or optical jumper.

15           The present invention may also be used to fabricate so-called "smart pixels". This is shown in FIG. 141-142. Conventional smart pixels integrate an array of VCSELs and photodetectors onto a chip in order to facilitate OE communication of a chip to other elements. However, conventional smart pixels are expensive to manufacture and have a low yield. As shown in FIG. 141, a polymer film (OE-film-D) with an array of VCSELs  
20       and photodetectors embedded in it may be used to achieve the same function as a smart pixel. Additional electrical pad connections to the chip may be made with vias. As shown in FIG. 142, a smart pixel may also be fabricated using an active OE film with integrated waveguides, (OE-film-DW). A "smart pixel" may be fabricated by embedding an array of photodetectors and VCSELs in a polymer film which may then be electrically  
25       coupled to a chip. The smart pixel of the present invention is substantially easier to fabricate than conventional smart pixels. An OE-film-D plays the same role as VCSEL/Photodetector array in a conventional chip-type smart pixel chip. The OE-film- has the advantage that comparatively expensive semiconductor devices are only placed where they are necessary in the OE-film-D. This may result in potential cost savings.

Additionally, the polymer film facilitates the processing of vias, pads, and electrical lines.

FIG. 135 shows an illustration of an embodiment in which there is both-side packaging. As shown in the cut-out side view of FIG. 135, a first passive waveguide substrate communicates optical signals to an OE backplane layer and hence to a second passive waveguide substrate. OE film substrates with active layers may be connected to both sides of the first and second passive waveguide substrates. This permits chips or MCMs to be coupled to both sides of each passive waveguide. As shown in the perspective view of FIG. 135, this facilitates a three-dimensional module. Preferably additional support members (not shown in FIG. 135) are used, as required, to provide the requisite mechanical strength to the three dimensional module.

The present invention may be extended to include OE printed circuit boards or mother boards. As shown in FIG. 143, an OE printed circuit board is preferably optically coupled to an OE MCM using forty-five degree mirror optical couplers, although other optical couplers could also be used. Electrical outputs in each chip control the VCSELs in each OE MCM. The emitted light of some of the VCSELs may be coupled to other chips (intra MCMs). However, the light from other VCSELs may be coupled to the OE PCB from the backside to the OE-film, permitting optical communication to other elements, such as other OE MCMs.

FIG. 144 shows a stacked OE film structure used for both intra-MCM and inter MCM optical connection. A first OE-film with optical emitters and detectors is used for intra-MCM optical interconnections. As shown in FIG. 144, the first film may, for example, optically interconnect four chips. The first OE-film is also coupled to a second OE-film. The second OE-film has passive waveguides that may be used for inter-MCM (e.g., inter-board) optical interconnections. As shown in FIG. 144, the second film may, for example, couple four four-chip MCMs on a board. Separate optimization of the waveguide dimensions of the first OE-film and the second (passive) OE film are possible. As shown in FIG. 144, the waveguides and couplers in the second passive film may, for example, have larger apertures corresponding to a large beam spot size. Preferably, the photodetector apertures are also correspondingly enlarge in accord with the beam spot

size of the waveguide coupler. Appropriate electrical connections are made by vias to electrical boards.

FIGS. 145 and 146 shows alternate embodiments of a stacked OE film structure used for both intra-MCM and inter-MCM (e.g., intra-board interconnections). As shown in FIGS. 145-146, the function of an active film incorporating waveguides, detectors, and optical emitters, may be implemented with a combination of passive waveguide films and active device films. This may, potentially, lead to a higher yield than the embodiment of FIG. 144.

In summary, the method of the present invention enables electronic devices and components and a wide variety of active and passive electro-optic devices to be embedded in a film in a manner consistent with the efficient optical transmission of signals to other electro-optic devices in an interposer, multi-chip module, or inter-multi-chip package. The method of the present invention may be generalized to fabricate a variety of passive waveguide film structures; films with embedded electro-optic and electrical devices; and films having both passive waveguides and active electro-optic devices. The ability to maintain the planarity of a single film and to extend vias and conventional Z connections through a signal film enables complex three-dimensional stacks of films to be fabricated. This flexibility is extremely useful in designing a high-yield, low cost, high-speed multi-chip module, substrate, optical link module, etc., to couple signals between a plurality of chips, CSPs, MCMs, or boards.

While the present inventions have been particularly described with respect to the illustrated embodiments, it will be appreciated that various alterations, modifications and adaptations may be made based on the present disclosure, and are intended to be within the scope of the present inventions. While the inventions have been described in connection with what is presently considered to be the most practical and preferred embodiments, it is to be understood that the present invention is not limited to the disclosed embodiments but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

**WHAT IS CLAIMED IS:**

1. A substrate having optical and electrical interconnections, comprising:
  - a first layer having polymeric waveguides formed therein;
  - a second layer having polymeric waveguides formed therein;
  - a first vertical optical coupler formed in said first layer and optically coupled to a
  - 5 first waveguide in said first layer;
  - a second vertical optical coupler formed in said second layer and optically
  - coupled to a second waveguide in said layer;
  - wherein said first optical coupler is positioned adjacent said second vertical
  - optical coupler so that light may be coupled between said first and said second
  - 10 waveguides.
2. The substrate of Claim 1 wherein at least a portion of said substrate is formed by a build-up process.
- 15 3. The main substrate of Claim 1 wherein at least a portion of said substrate is formed by a lamination process.
4. The main substrate of Claim 1 further comprising:
  - at least one additional layer having polymeric waveguides formed therein;
  - 20 an additional vertical optical coupler formed in said at least one additional layer
  - and optically coupled to a waveguide in said at least one additional layer;
  - wherein said layers are stacked face-to-face and are optically coupled by said
  - vertical optical couplers.
- 25 5. The substrate of Claim 4, wherein at least a portion of said substrate is formed by a build-up process.
6. The substrate of Claim 4, wherein at least a portion of said substrate is formed



by a lamination process.

7. The substrate of Claim 1 wherein said vertical optical couplers are coated with anti-reflective layers.

5

8. The substrate of Claim 1 wherein external light is coupled to a waveguide in at least one of said layers using an optical connector selected from the group consisting of optical fibers, film waveguide arrays, image guides, or fiber arrays.

10

9. The substrate of Claim 1 wherein at least one waveguide in said first layer has a first portion whose length is parallel to the first layer's surfaces, and a second portion whose length is perpendicular to the first layer's surfaces, wherein each waveguide portion has a first end and a second end, wherein the first ends of said waveguide portions are optically coupled to one of said vertical optical couplers, and wherein the second end of said second waveguide portion extends to a surface of said first layer.

15

10. The substrate of Claim 1 wherein said first layer has waveguides integrally formed with a plurality of opto-electronic devices.

20

11. The substrate of Claim 10 wherein at least a portion of said substrate is formed by a build-up process.

12. The substrate of Claim 10 wherein at least a portion of said substrate is formed by a lamination process.

25

13. The substrate of Claim 10, wherein external light is coupled to a waveguide in at least one of said layers using an optical connector selected from the group consisting of optical fibers, film waveguide arrays, image guides, or fiber arrays.

14. The substrate of Claim 4 wherein at least one of said layers has a plurality of waveguides which are integrally formed with a plurality of opto-electronic devices.

5 15. The substrate of Claim 14 wherein at least a portion of said substrate is formed by a build-up process.

16. The substrate of Claim 14 wherein at least a portion of said substrate is formed by a lamination process.

10 17. The substrate of Claim 14, wherein external light is coupled to a waveguide in at least one of said layers using an optical connector selected from the group consisting of optical fibers, film waveguide arrays, image guides, or fiber arrays.

15 18. The substrate of Claim 10 wherein at least one waveguide in one of said layers has a first portion whose length is parallel to the layer's surfaces, and a second portion whose length is perpendicular to the layer's surfaces, wherein each waveguide portion has a first end and a second end, wherein the first ends of said waveguide portions are optically coupled to one of said vertical optical couplers, and wherein the second end of said second waveguide portion extends to a surface of said layer.

20

19. A substrate having optical and electrical interconnections, comprising:  
a first polymer layer having polymer waveguides formed therein; and  
a second polymeric layer having a plurality of optoelectronic devices integrally formed therein;

25

wherein the layers are laminated to one another to form a stack of layers.

20. The substrate of Claim 19 wherein at least one of the opto-electronic devices is selected from the group consisting of a VCSEL, a VCSEL with driver circuit, a photodetector, a photodetector with amplifier circuit, a light modulator, an optical switch,

a lens, a mirror, a LED, a light amplifying film, a semi-transparent mirror, a grating, a high refractive index element, a driver chip, and amplifier chip, a wavelength filter, a tunable filter, a wavelength converter, a resistor, a capacitor, a mini-chip, and a waveguide.

5

21. The substrate of Claim 19 wherein the opto-electronic device includes a driver for a VCSEL.

10 22. The substrate of Claim 19 wherein the opto-electronic device includes at least one photodetector and at least one pre-amplifier.

23. The substrate of Claim 22 further comprising a resistor coupling the output of said amplifier to said photodetector.

15 24. The substrate of Claim 19 further comprising a photodetector and a resistor coupled the output of said photodetector.

20 25. The substrate of Claims 19 wherein the polymeric waveguide layer comprises multiple dielectric layers.

26. The substrate of Claim 19 further comprising:  
a third polymeric layer having a plurality of electronic integrated circuit chips integrally formed therein; and  
wherein the layers are laminated to one another to form a stack of layers.

25

27. The substrate of Claim 26 wherein at least one of the opto-electronic devices comprises at least one of the following devices: a VCSEL, a VCSEL with driver circuit, a photodetector, a photodetector with amplifier circuit, a light modulator, an optical switch, a lens, a mirror, a LED, a light amplifying film, a semi-transparent mirror, a grating, a

high refractive index element, a driver and amplifier chip, optical amplifier, wavelength filter, tunable filter, wavelength converter, resistor, capacitor, mini-chip, and a waveguide.

5           28. The substrate of Claim 27 wherein the opto-electronic device comprises a VCSEL and a driver circuit.

29. The substrate of Claim 26 wherein the opto-electronic devices comprises a photodetector with an amplifier.

10

30. The substrate of Claim 29 further comprising a resistor coupling the input of said amplifier to said photodetector.

15

31. The substrate of Claim 27 wherein the electronic integrated circuit chips comprises at least one of a driver for a VCSEL and an amplifier for a photodetector.

20

32. The substrate of Claim 26 wherein one of said opto-electric devices comprises a photodetector, and wherein said substrate further comprising a resistor which couples a pad of an electronic integrated circuit chips to said photodetector.

33. The substrate of Claim 19 wherein at least a portion of the substrate is formed by a build-up process.

25

34. A substrate comprising:  
a first board with vertically oriented optical switch devices and micro-lenses disposed at their optical outputs;  
a second board with vertically oriented photo-detector devices and micro-lenses disposed at their optical inputs; and  
wherein the boards are disposed opposite to one another so that corresponding

switch devices and photo-detector devices are aligned to one another.

35. An optical interconnect system for communicating information between a plurality of chips, comprising:

5                   a first opto-electronic multichip module having a top surface for mounting chips and a bottom film layer with at least one waveguide configured to couple optical signals into and out of said opto-electronic multi-chip module;

                  a second opto-electronic multichip module having a top surface for mounting chips and a bottom film layer with at least one waveguide configured to couple  
10                  optical signals into and out of said opto-electronic multi-chip module;

                  at least one passive film with an optical waveguide layer disposed proximate said bottom surfaces of said first and second multi-chip modules and coupling optical signals between said first and second multi-chip modules.

15                  36. The optical interconnect system of Claim 35, where said opto-electronic multichip modules comprise a stack of at least two film layers.

                  37. The optical interconnect system of Claim 36, wherein at least one of the film layers is a passive waveguide film and the other film is an active device film having  
20                  detectors, and light emitters and/or light modulators.

                  38. The optical interconnect system of Claim 36, wherein one of the film layers is an electrical layer.

25                  39. The optical interconnect system of Claim 35, further comprising a passive optical backplane waveguide layer to optically couple eletro-optic multichip modules disposed on opposite sides of said backplane waveguide layer.

                  40. The optical interconnect system of Claim 35, further comprising a passive

optical motherboard waveguide layer to optically couple eletro-optic multichip modules disposed on opposite sides of said motherboard waveguide layer.

- 5        41. An electro-optic module for communicating optical signals between at least two electrical circuit terminals, comprising:
- at least one substrate, wherein each substrate is selected from the group consisting of substrates with passive polymer waveguides, substrates with electro-optic elements embedded in a polymer film, substrates having embedded electrical elements, and substrates having passive polymer waveguides and embedded electrical and electro-optic
- 10        elements;
- optical waveguide means in at least one of the substrates for propagating optical signals;
- optical signal source means in at least one of the substrates for generating optical signals in at least one of the substrates; and
- 15        optical detection means in at least one of the substrates for detecting optical signals.

42. The module of Claim 41, further comprising:
- stack optical waveguide coupling means to communicate optical signals between
- 20        said plurality of substrates.

43. The module of Claim 41, further comprising:
- at least one electrical board; and
- via means for making electrical connections.

25

44. The module of Claim 41, further comprising: flexible coupling means for coupling optical energy to at least one waveguide of a substrate containing waveguides.

45. An electro-optic module for communicating optical signals between at least

two electrical circuit terminals, comprising:

at least one substrate, wherein each substrate is selected from the group consisting of substrates with passive polymer waveguides, substrates with electro-optic elements embedded in a polymer film, substrates having embedded electrical elements, and

5 substrates having passive polymer waveguides and embedded electrical and electro-optic elements;

optical waveguide means in at least one of the substrates for propagating optical signals;

10 optical switch means in at least on of the substrates for switching optical power or an optical signal in at least one of the substrates.

46. The module of Claim 45, further comprising:

stack optical waveguide coupling means to communicate optical signals between said plurality of substrates.

15

47. The module of Claim 47, further comprising:

at least one electrical board; and

via means for making electrical connections.

20

48. The module of Claim 45, further comprising: flexible coupling means for coupling optical energy to at least one waveguide of a substrate containing waveguides.

49. A method of making a substrate comprising the steps of:

25 separately manufacturing waveguide layers, IC chip layers, and opto-electric layers, each layer having at least one electrical via formed therein; and

laminating the layers together such that at least one electrical connection is made between two different layers, and such that the end of a waveguide in one layer is aligned to an opto-electric device in an adjacent layer.

**DECLARATION FOR PATENT APPLICATION**

As a below named joint inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**MULTI-LAYER OPTO-ELECTRONIC SUBSTRATES WITH ELECTRICAL AND  
OPTICAL INTERCONNECTIONS AND METHODS FOR MAKING**

the specification of which (check one)

- (X) is attached hereto.  
( ) was filed by an authorized person on my behalf on  
\_\_\_\_\_ as Application Serial No. \_\_\_\_\_  
and was amended on \_\_\_\_\_.  
(if applicable)

We hereby state that we have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

We acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Sect. 1.56(a).

We hereby claim foreign priority benefits under Title 35, United States Code, Sect. 119 of any foreign application(s) for patent or inventor's certificate listed below and so identified, and we have also identified below any foreign application for patent or inventor's certificate on this invention filed by me or my legal representatives or assigns and having a filing date before that of the application on which priority is claimed.

<u>Number</u>	<u>Country</u>	<u>Day/Month/Year Filed</u>	<u>Priority Claimed (Yes or No)</u>
NONE			



We hereby claim the benefit under Title 35, United States Code, Sect. 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sect. 112, we acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Sect. 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

<u>Application Serial No.</u>	<u>Filing Date</u>	<u>Status</u>
	NONE	

We hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below:

<u>Application Serial No.</u>	<u>Filing Date</u>
60/103,726	October 9, 1998

We hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

We hereby appoint the following attorneys, with full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent Office connected therewith and request that all correspondence and telephone calls in respect to this application be directed to COUDERT BROTHERS, 4 Embarcadero Center, Suite 3300, San Francisco, California 94111, Telephone No. (415) 986-1300:

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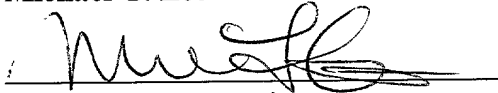
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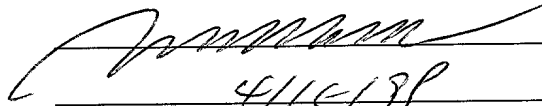
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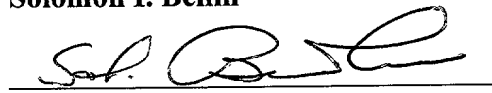
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Date:

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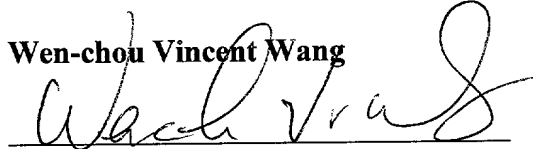
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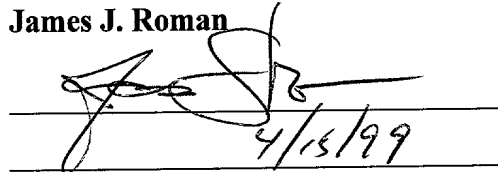
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**James J. Roman**  
  
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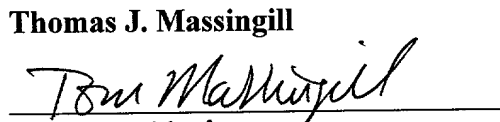
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**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Yoshimura, *et al.* )  
Serial No.: Unassigned )  
Filed: herewith on April 20, 1999 )  
For: MULTI-LAYER OPTO-ELECTRONIC )  
SUBSTRATES WITH ELECTRICAL )  
AND OPTICAL INTERCONNECTIONS )  
AND METHODS FOR MAKING )  
Art Unit: Unknown )  
Examiner: Unknown )

**CERTIFICATE OF MAILING**  
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HAL R. YEAGER  
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(Signature of person mailing)

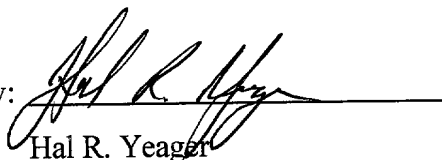
**COMMUNICATION UPON FILING**

Hon. Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

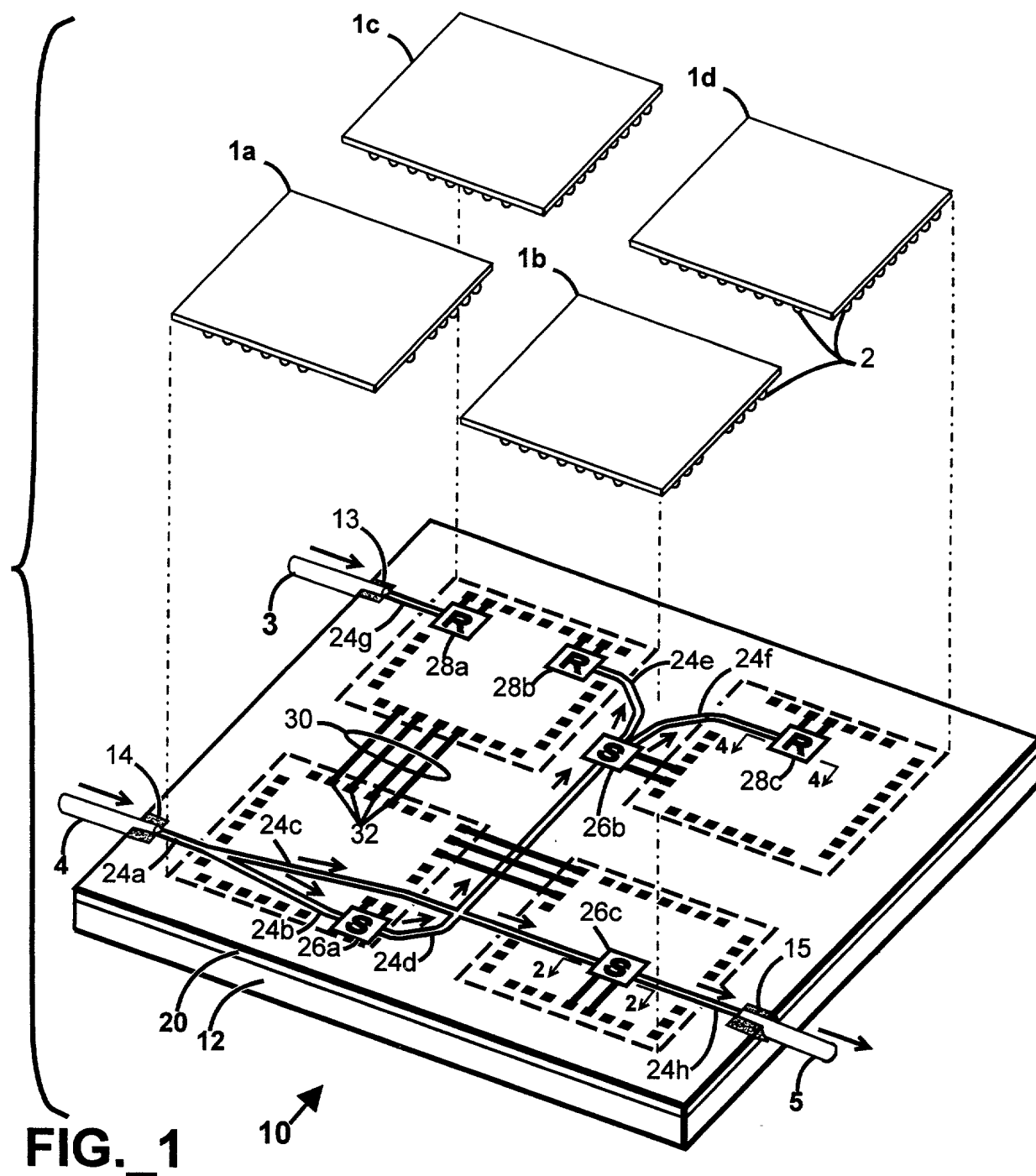
Attached herewith are draft formal drawing for FIGS. 74-76, and 90-108 for better clarity  
of the informal FIGS. 74-76 and 90-108 attached to the filed application.

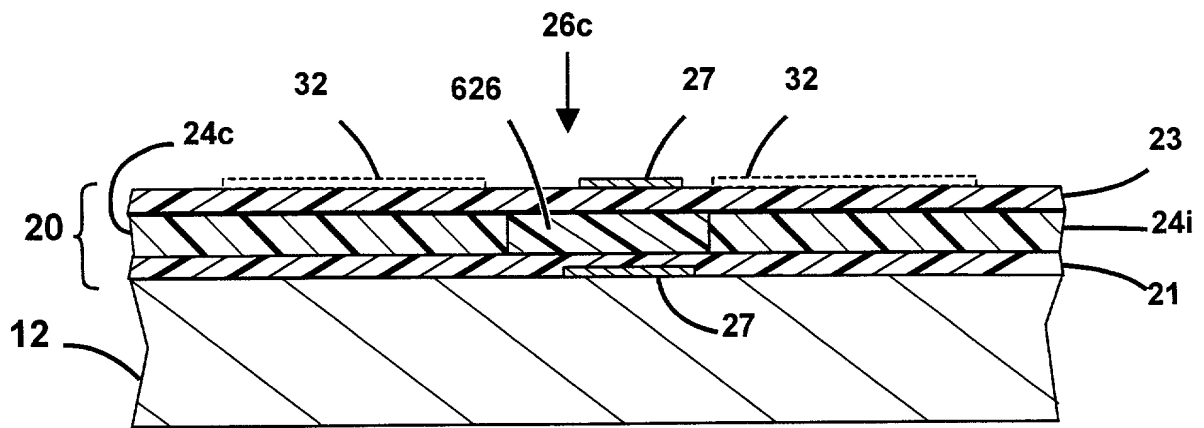
Respectfully submitted,

By:   
Hal R. Yeager

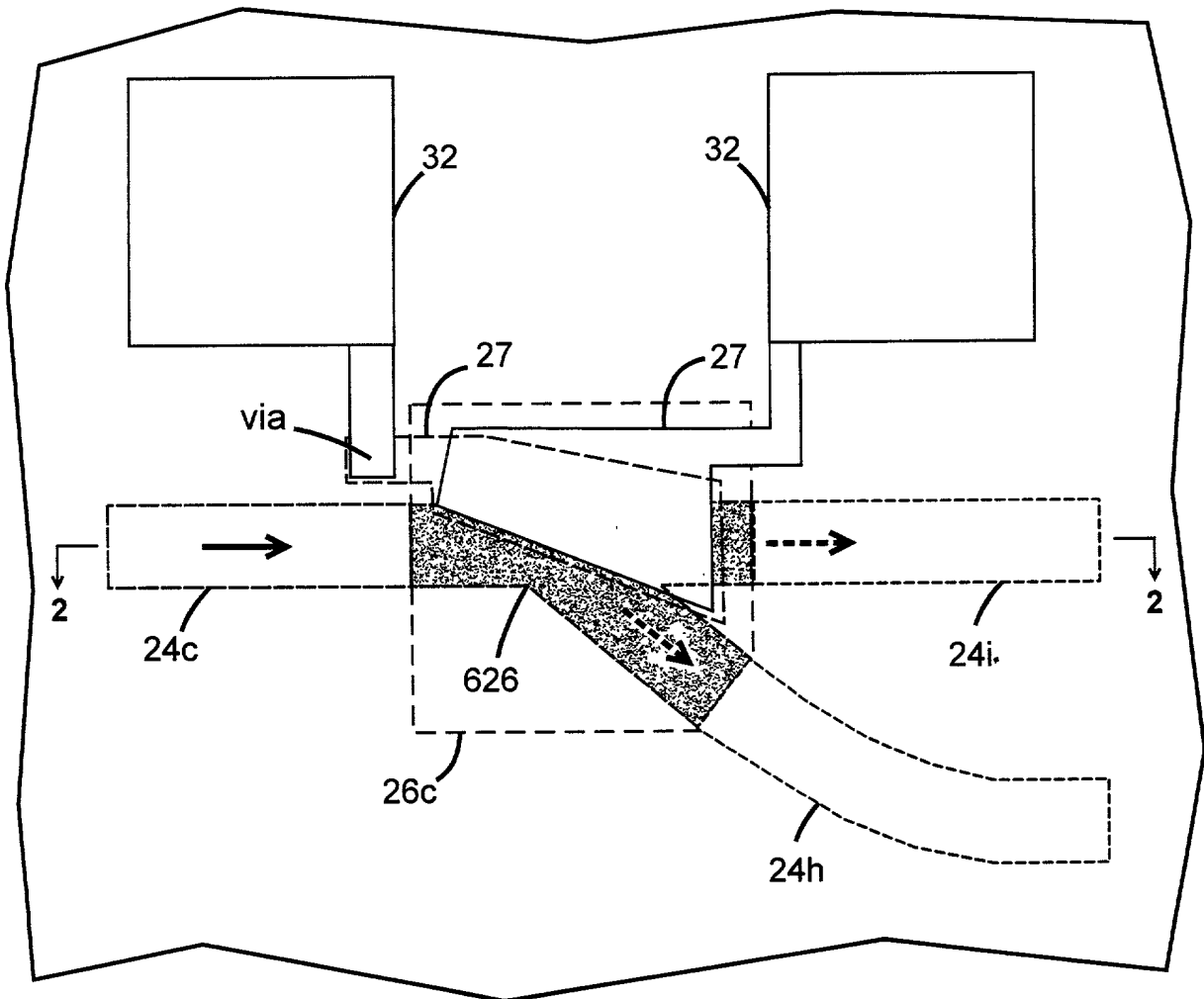
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**FIG.\_2**



**FIG.\_3**





28c'

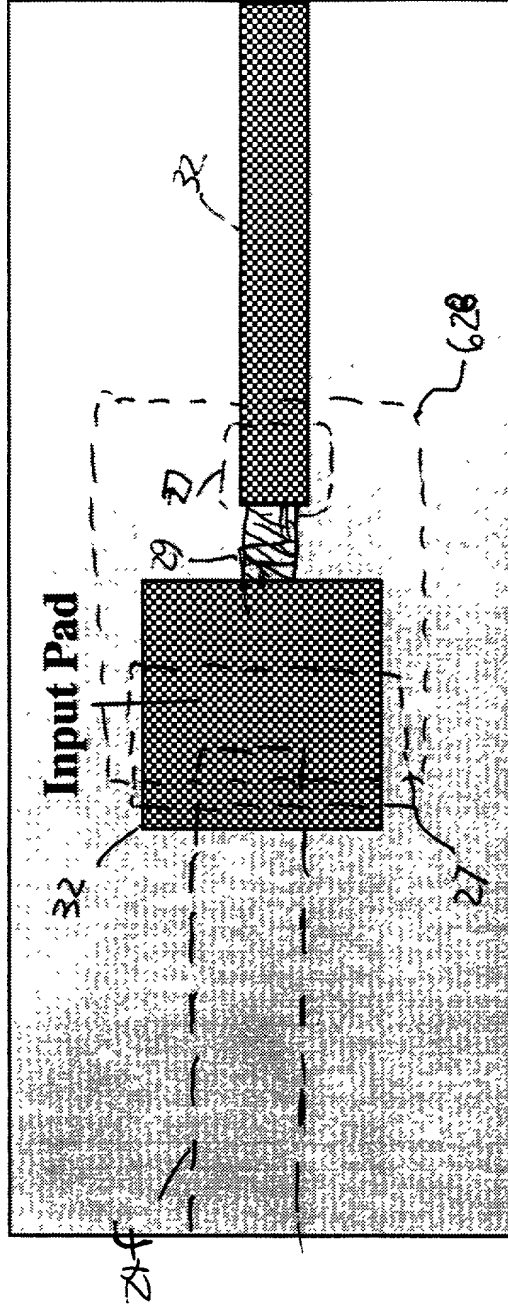


FIG. 5-2

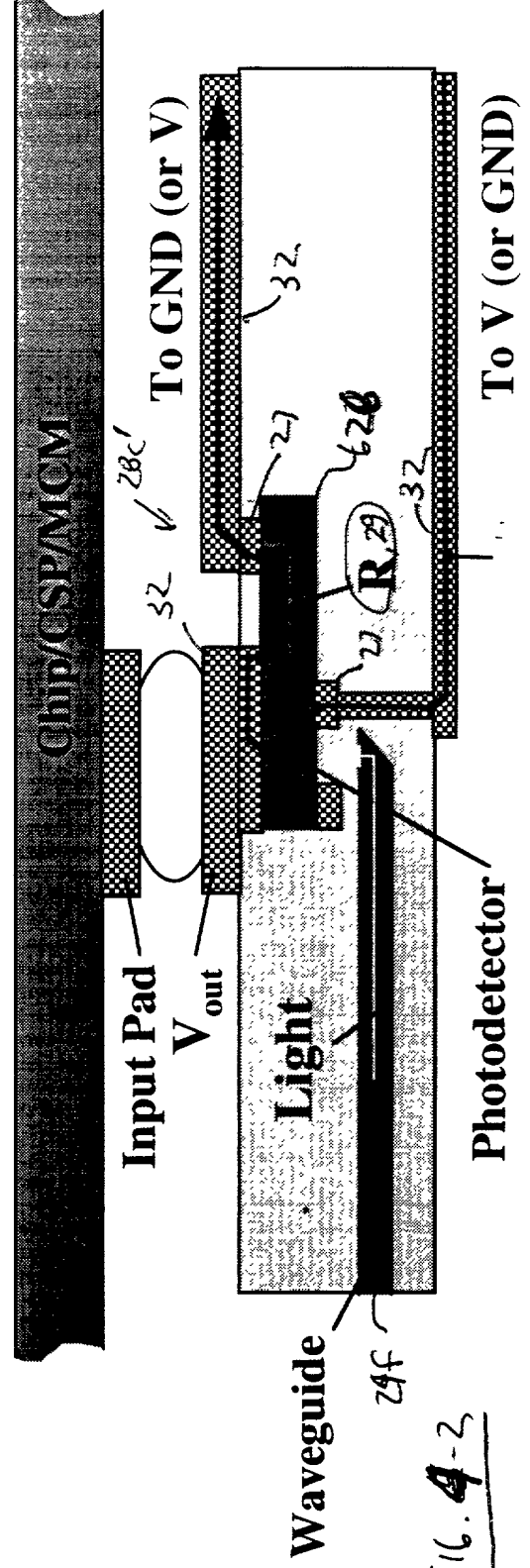


FIG. 4-2

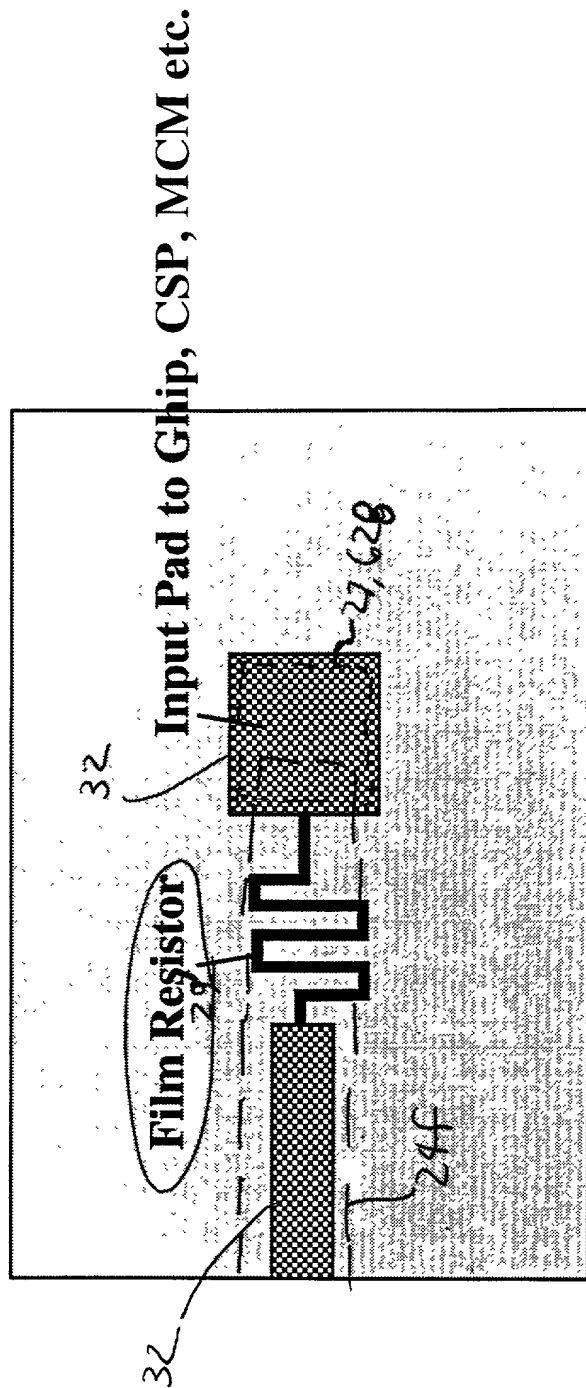


FIG. 5-3

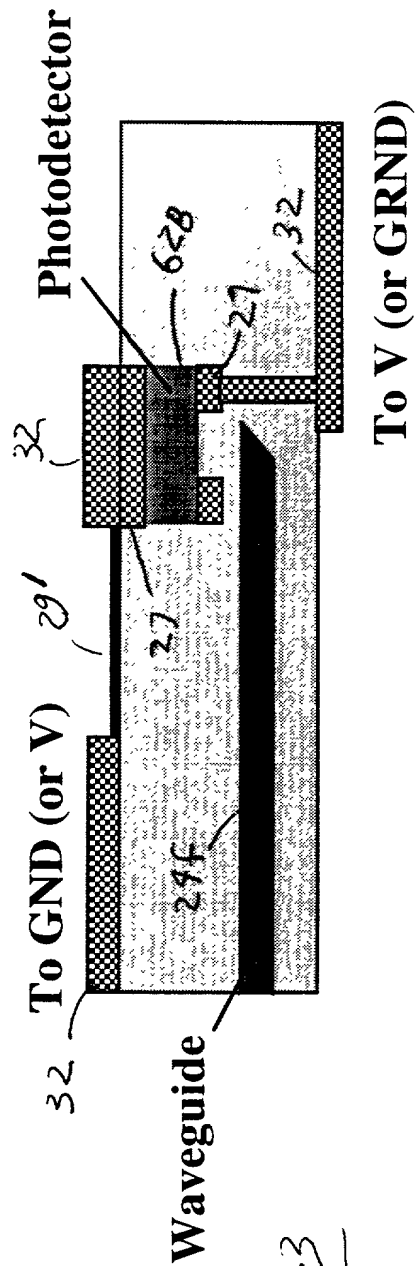


FIG 4-3

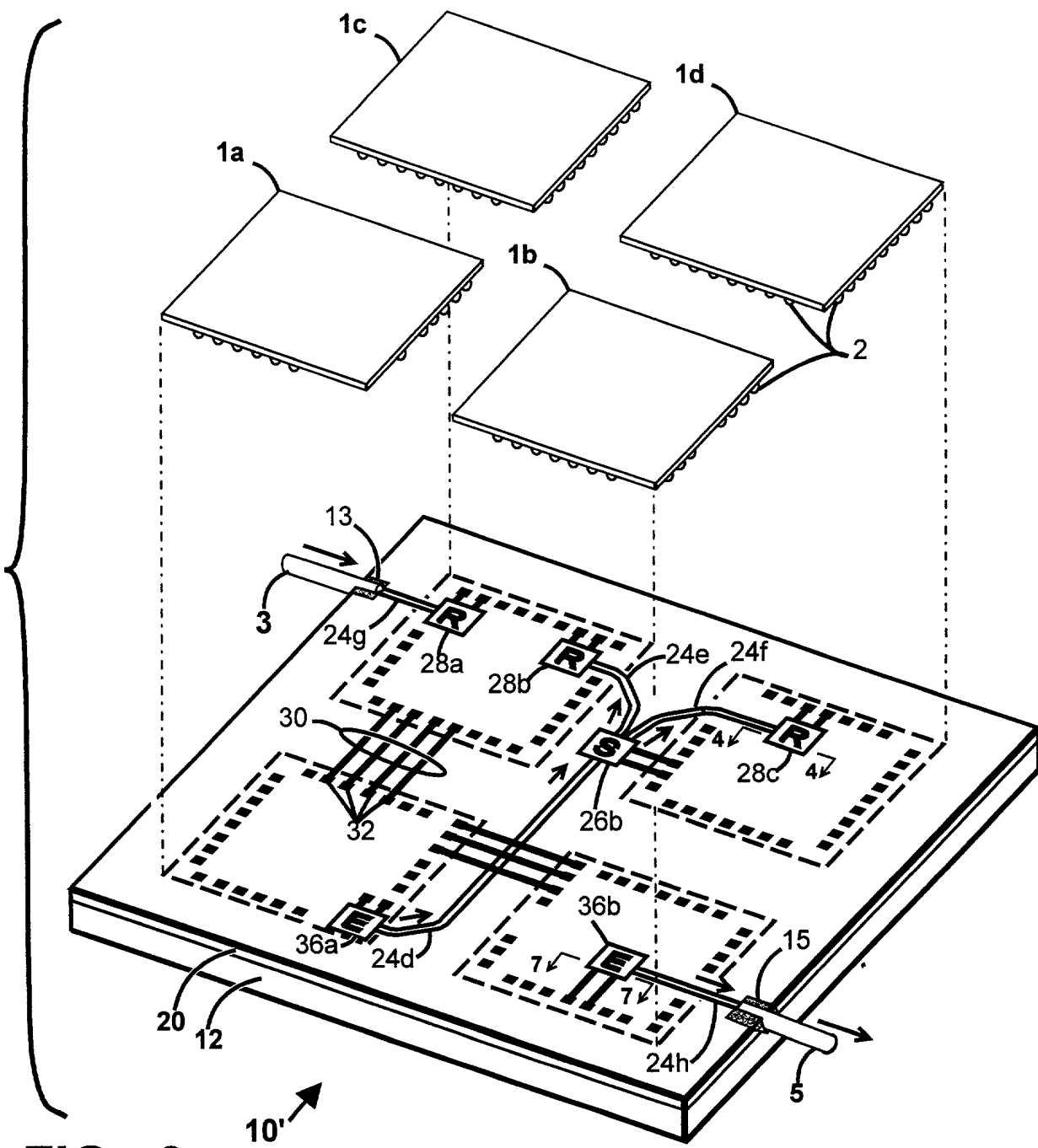
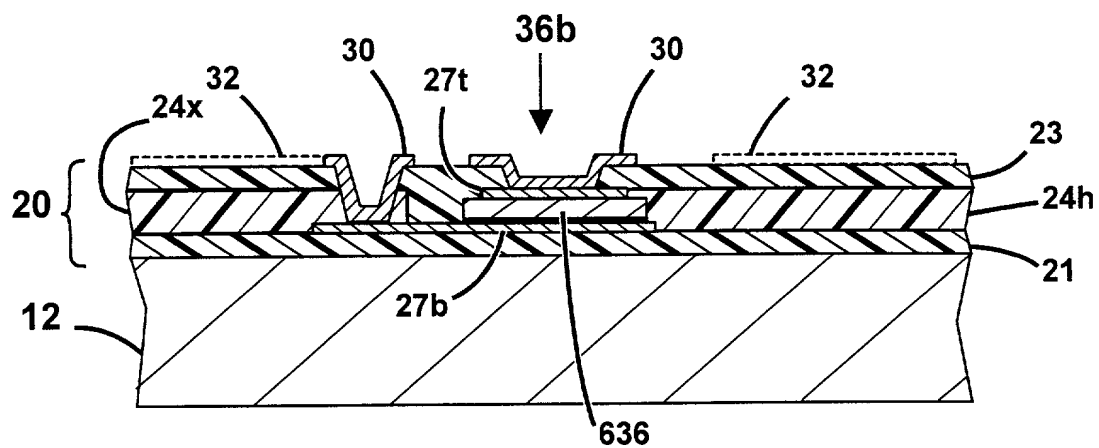
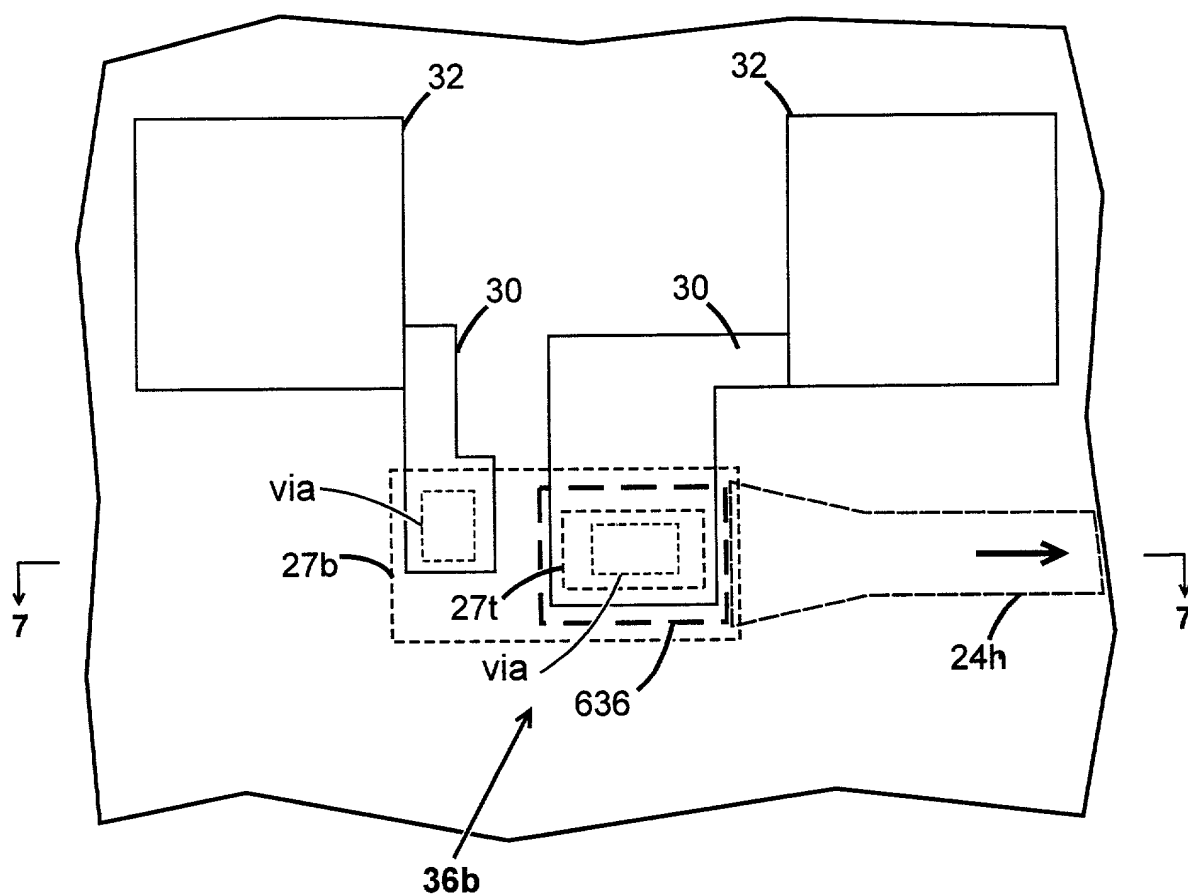


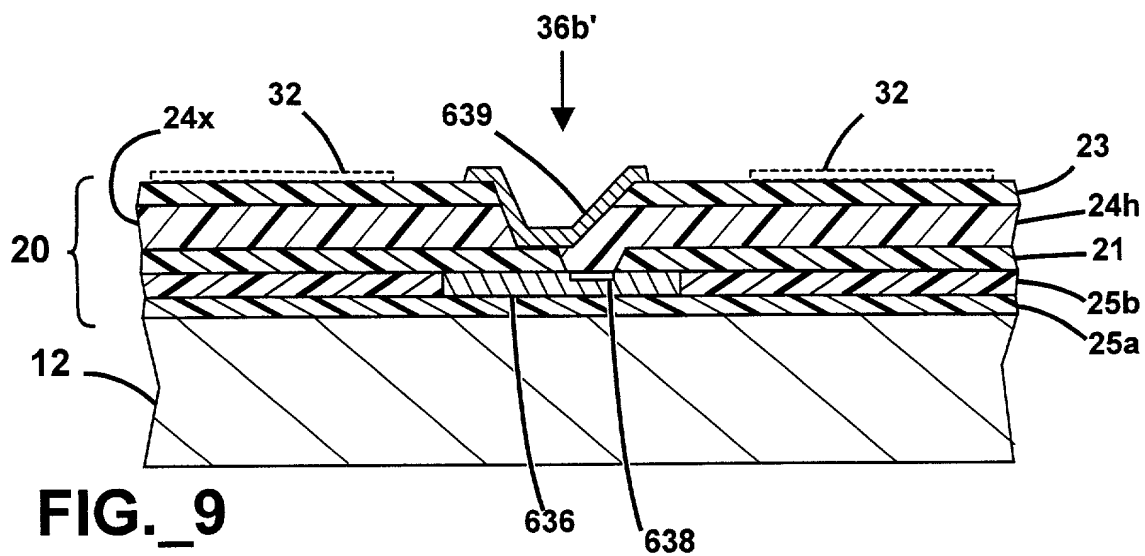
FIG.\_6



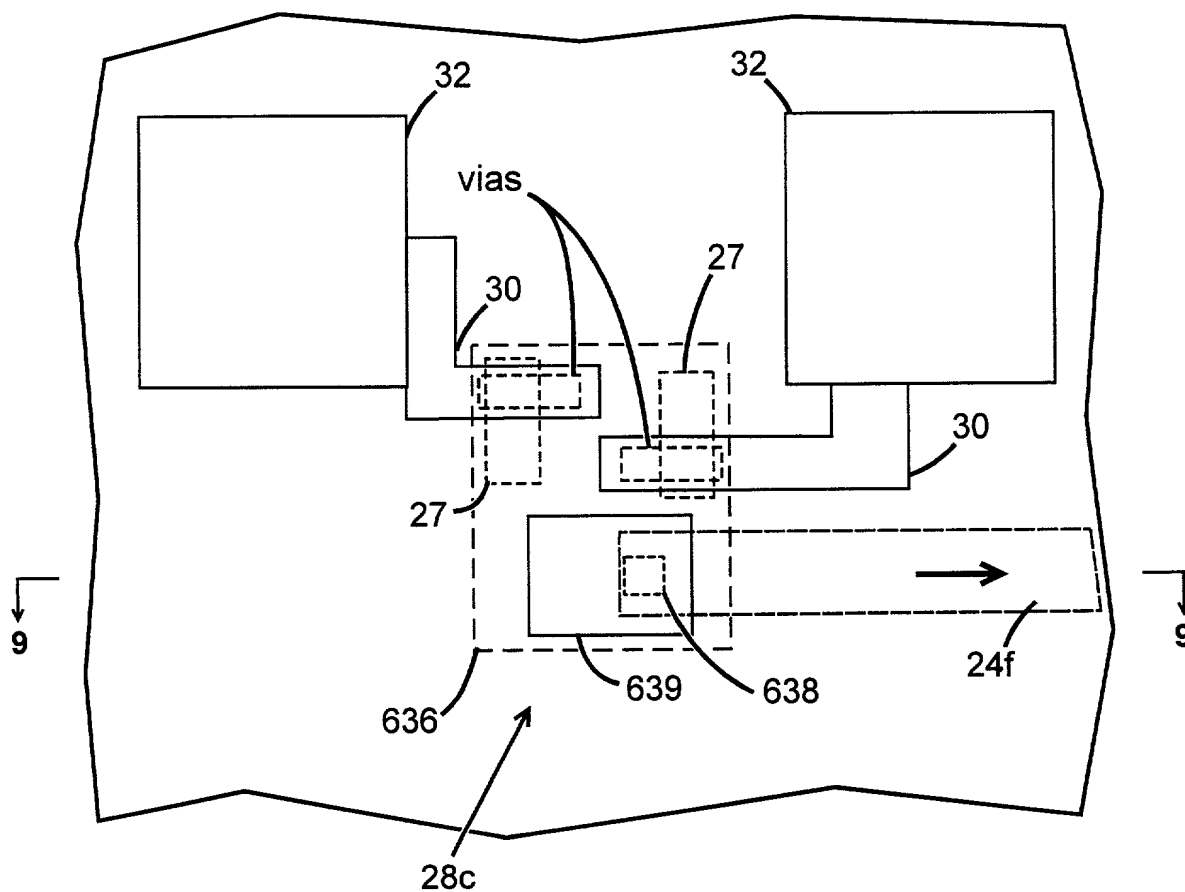
**FIG.\_7**



**FIG. 8**



**FIG. 9**



**FIG.\_10**

FIG.\_11

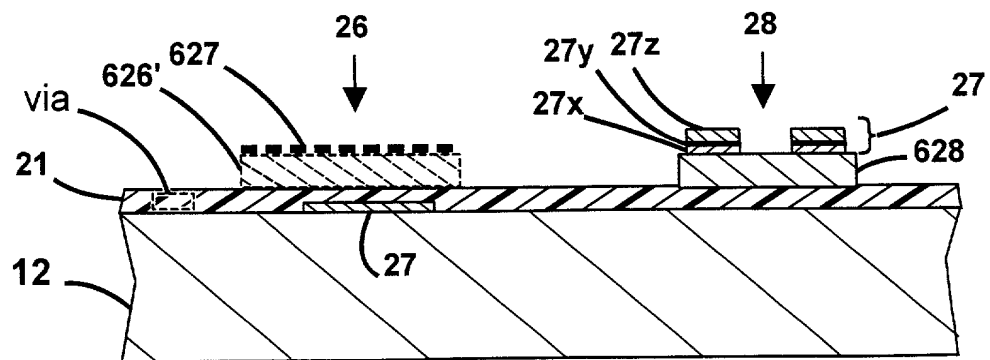


FIG.\_12

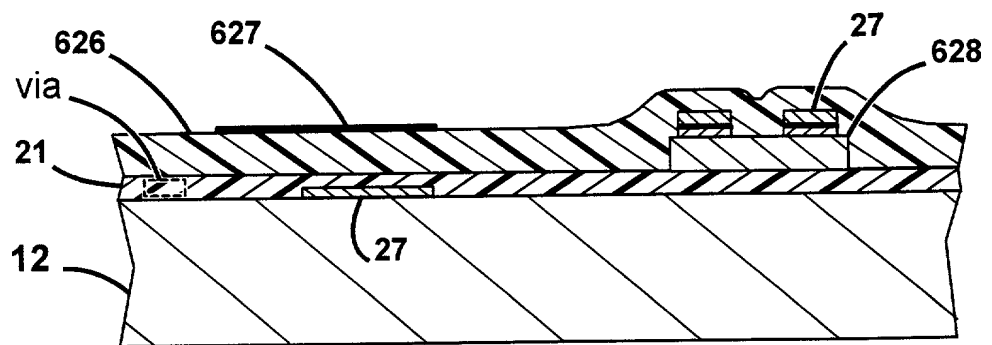


FIG.\_13

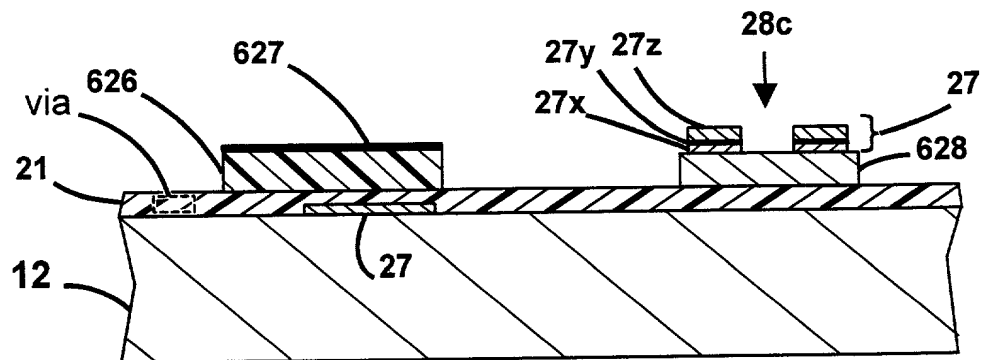


FIG.\_14

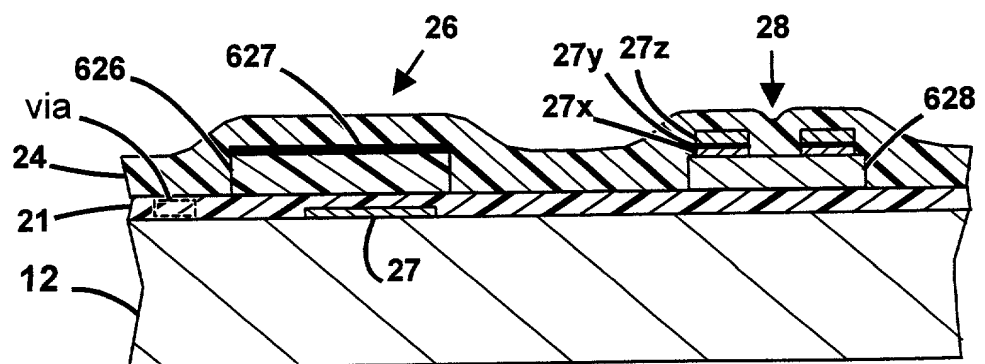


FIG.\_15

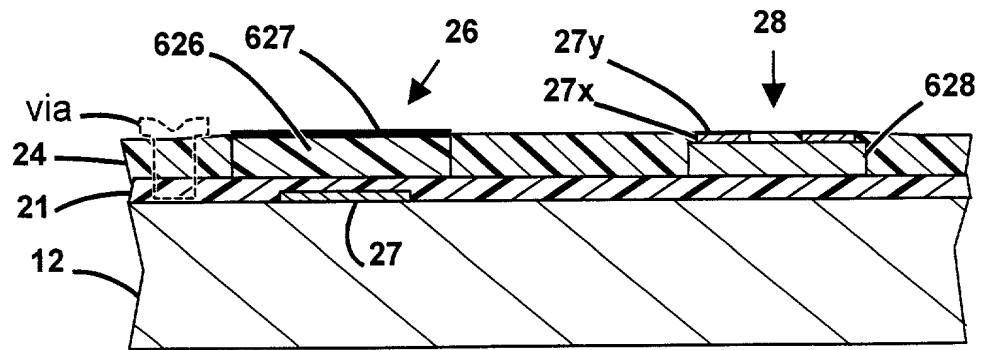


FIG.\_16

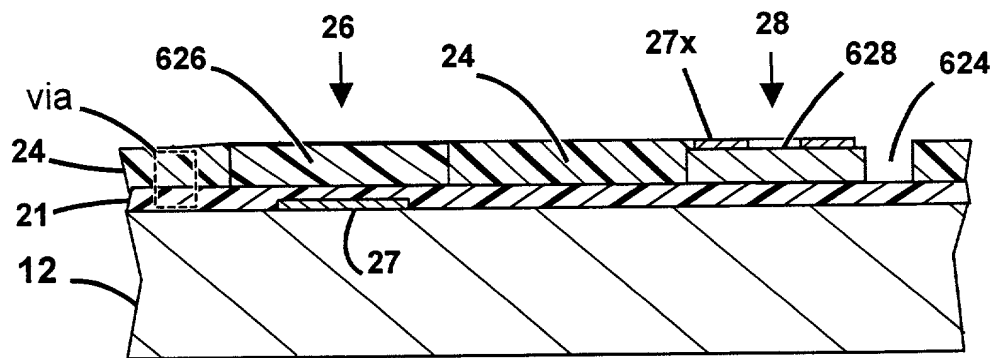


FIG.\_17

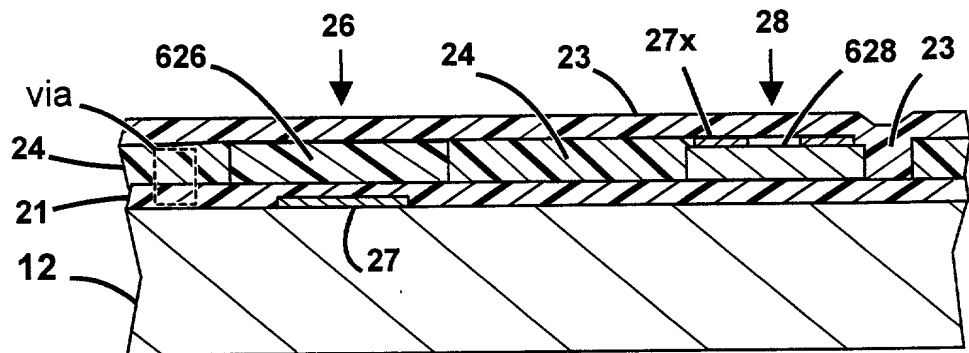
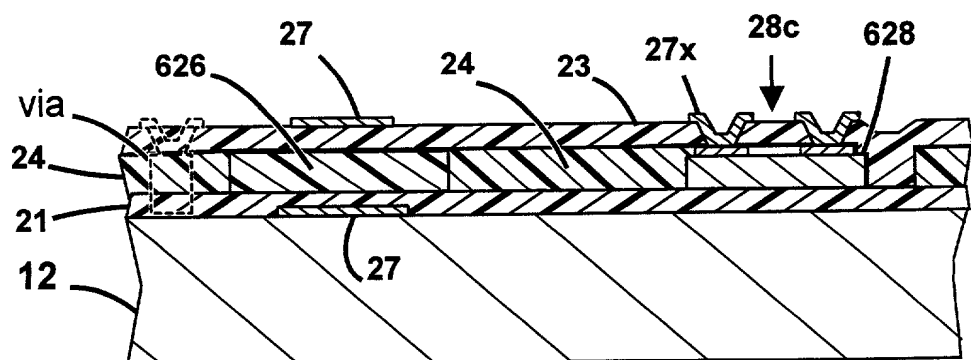


FIG.\_18



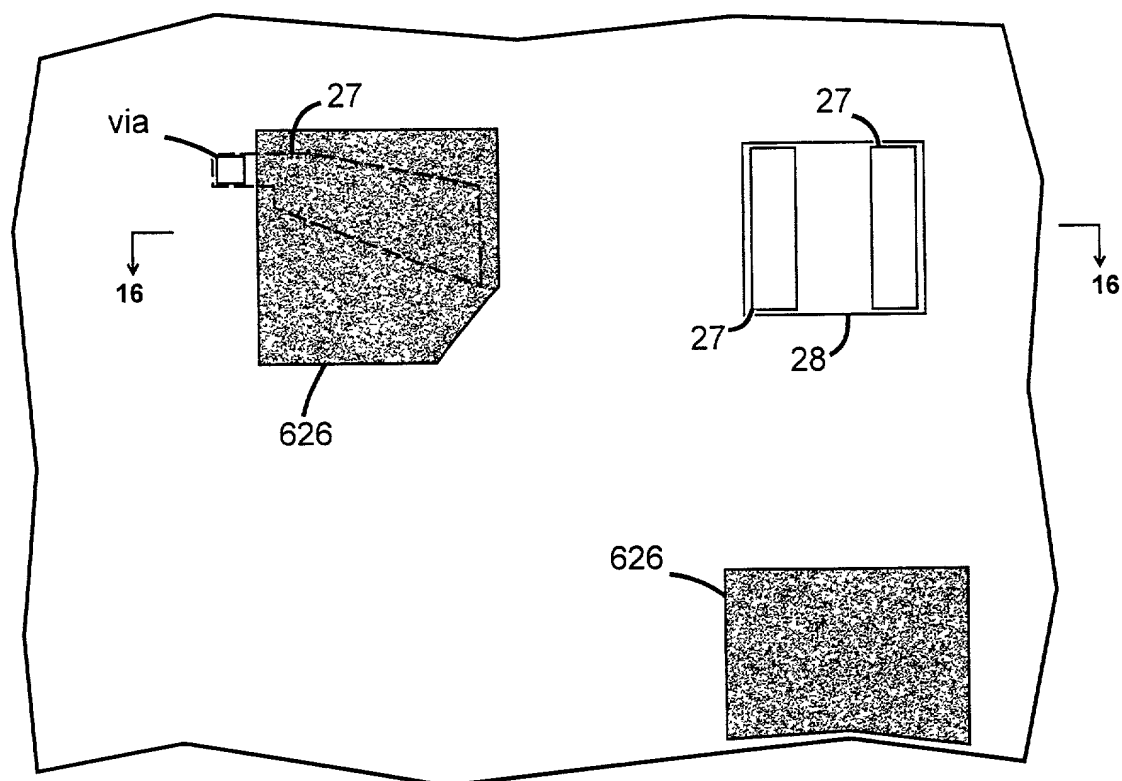


FIG.\_19

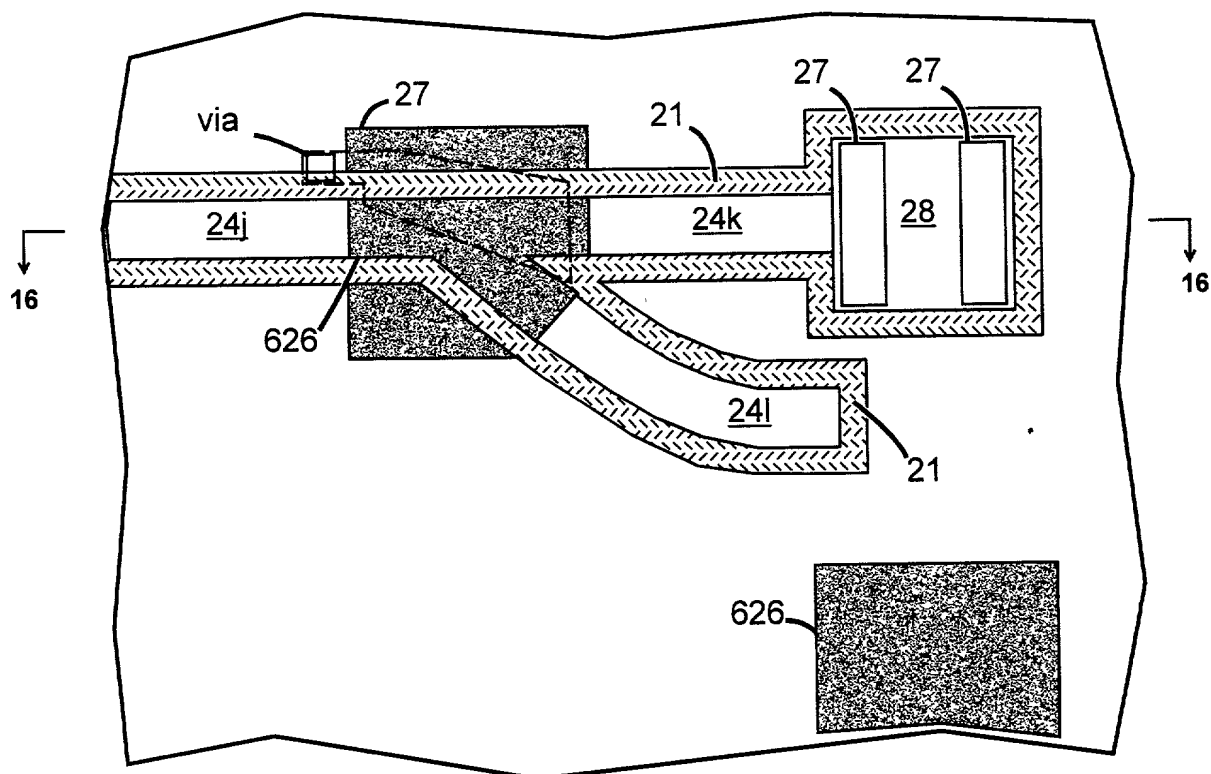


FIG.\_20



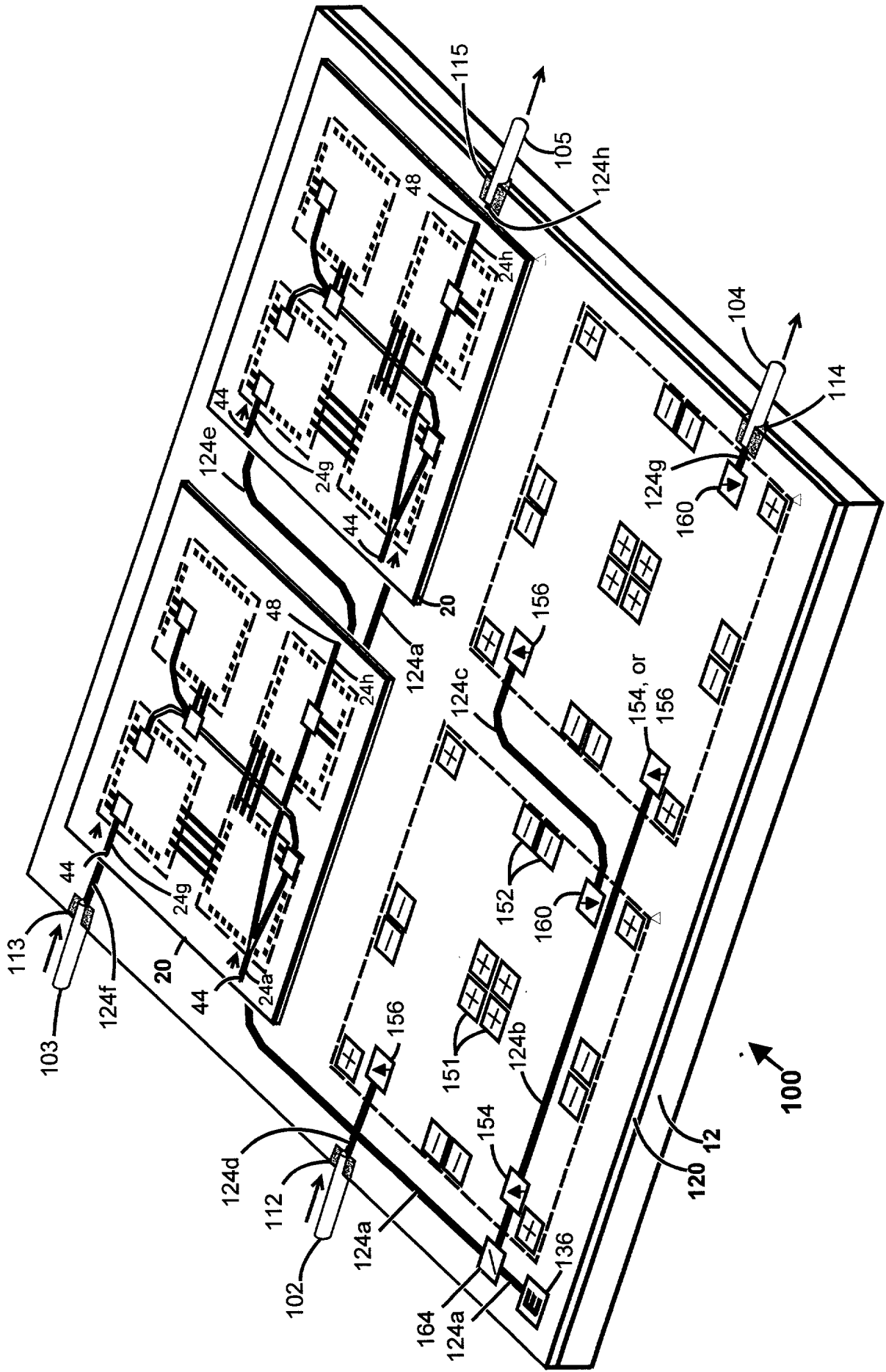


FIG. 21

600407 16446660

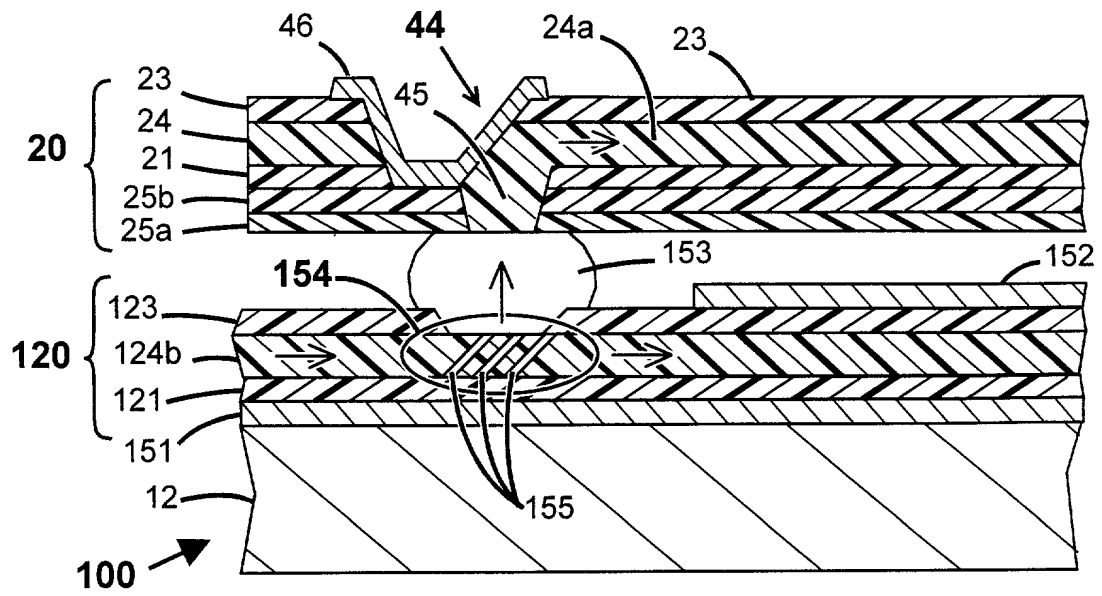


FIG.\_22

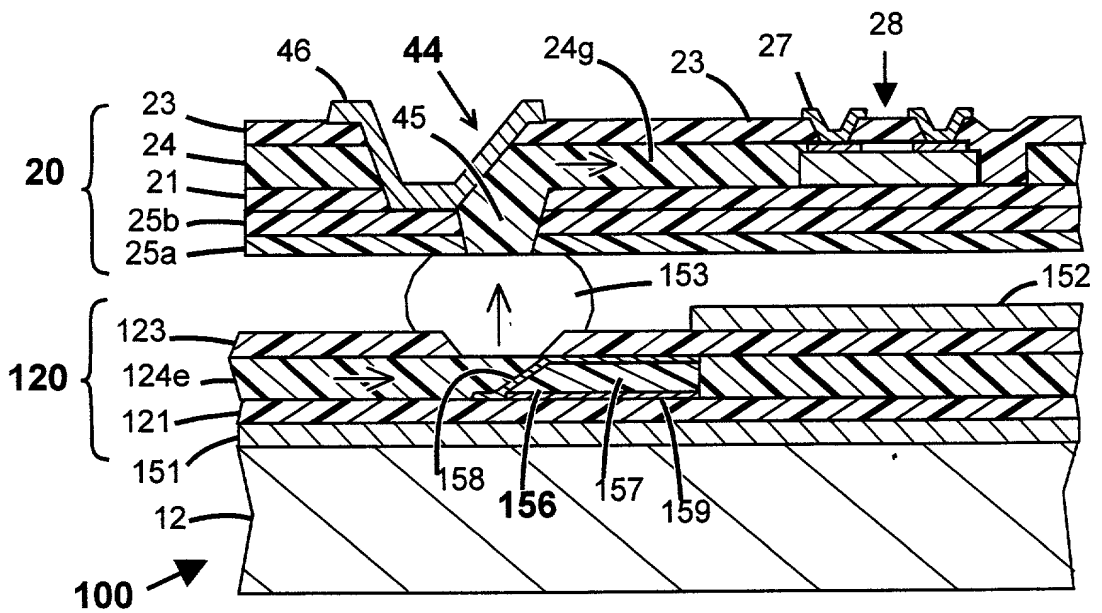
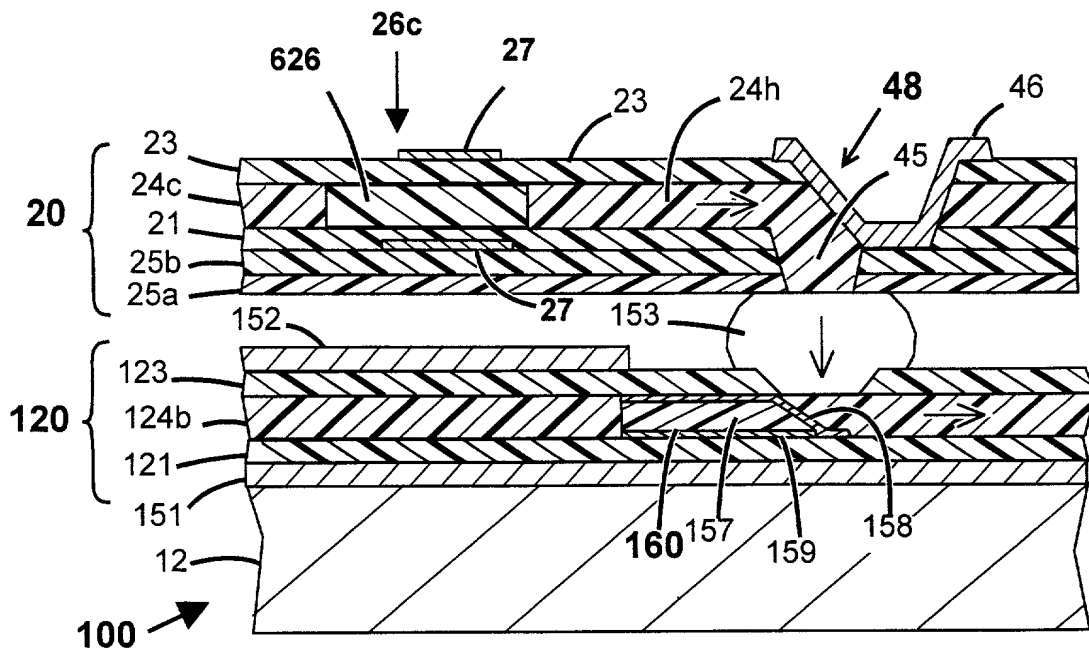
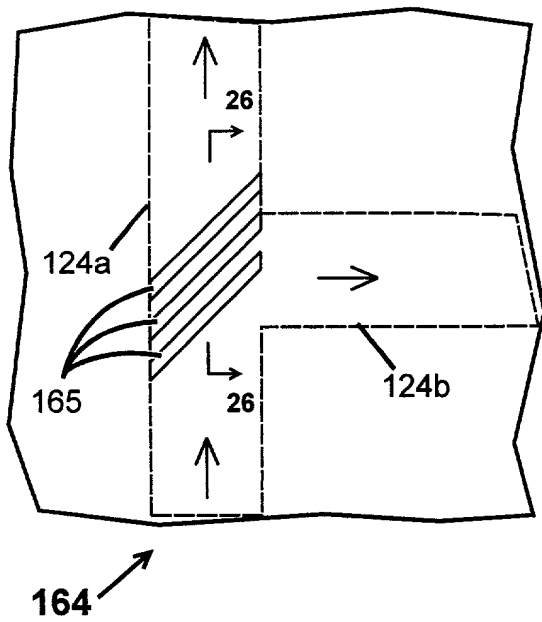


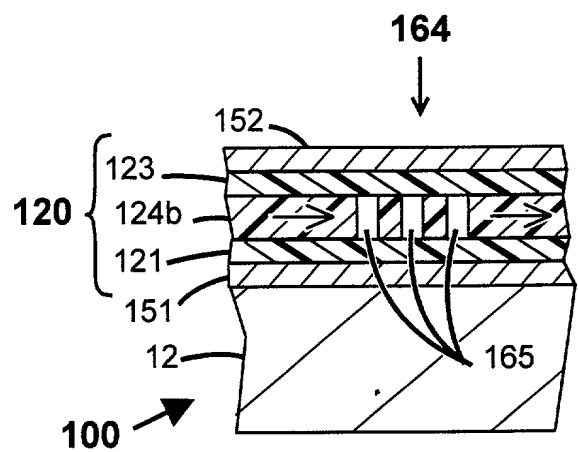
FIG.\_23



**FIG. 24**



**FIG. 25**



**FIG. 26**

FIG.\_27

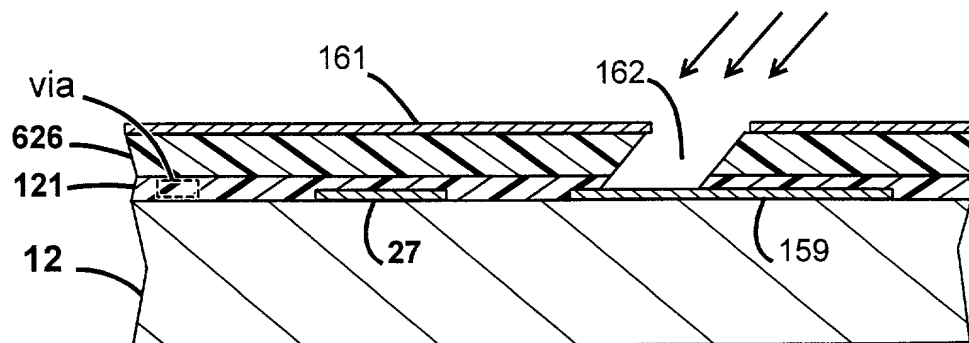


FIG.\_28

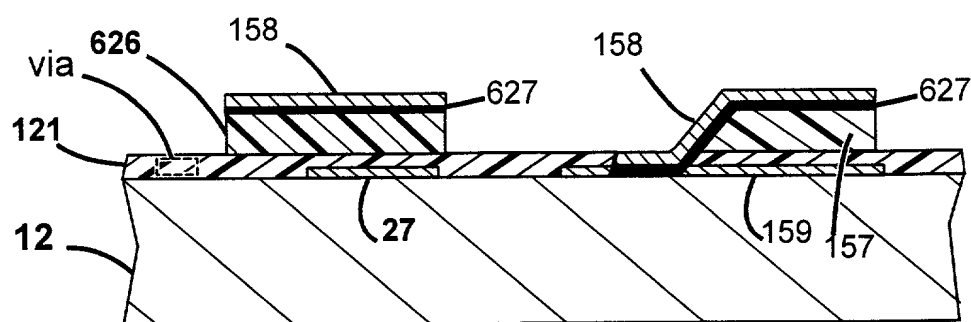


FIG.\_29

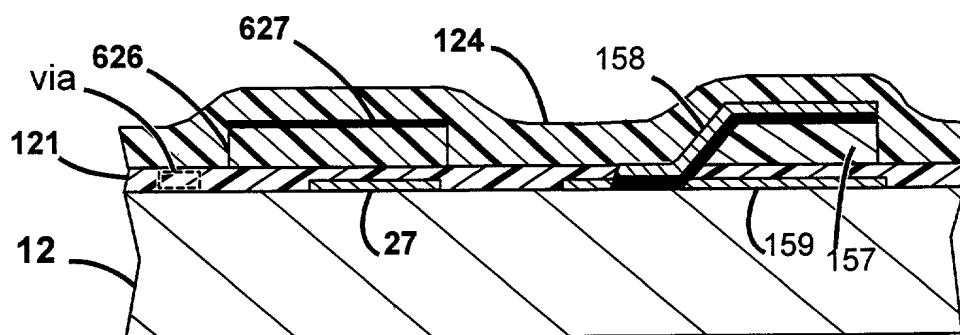
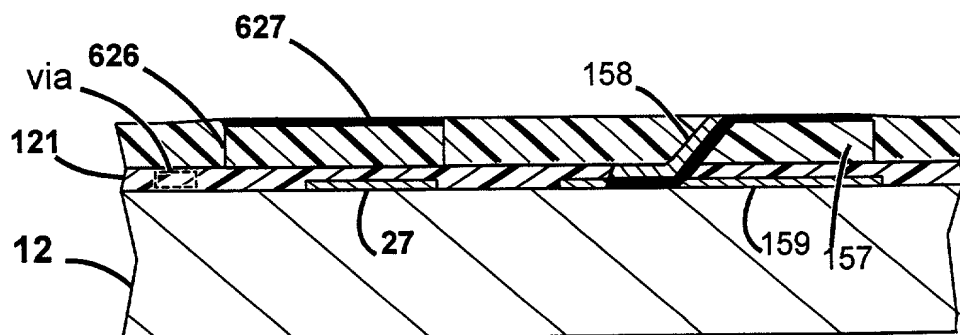
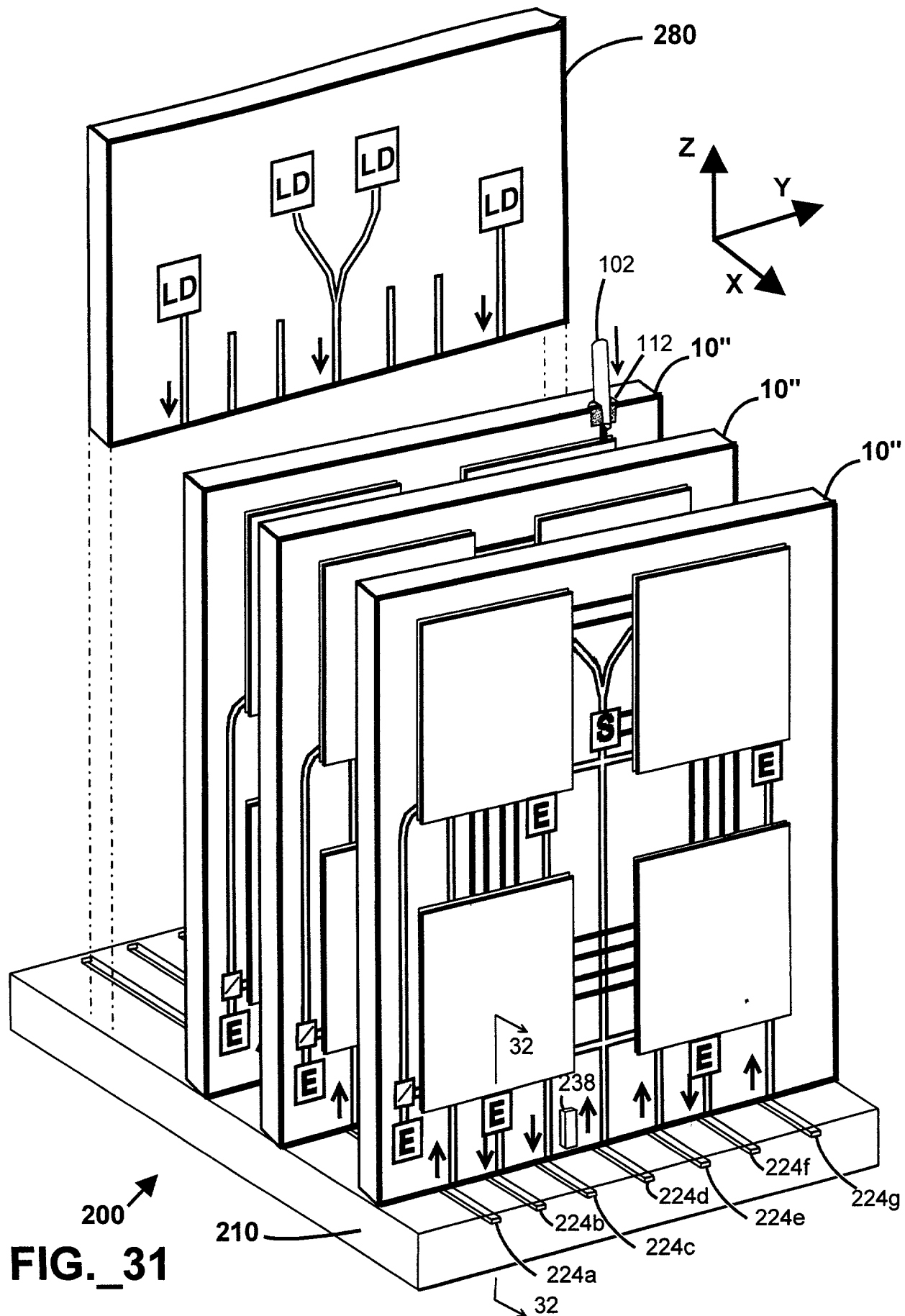


FIG.\_30



660663 744560



**FIG. 32**

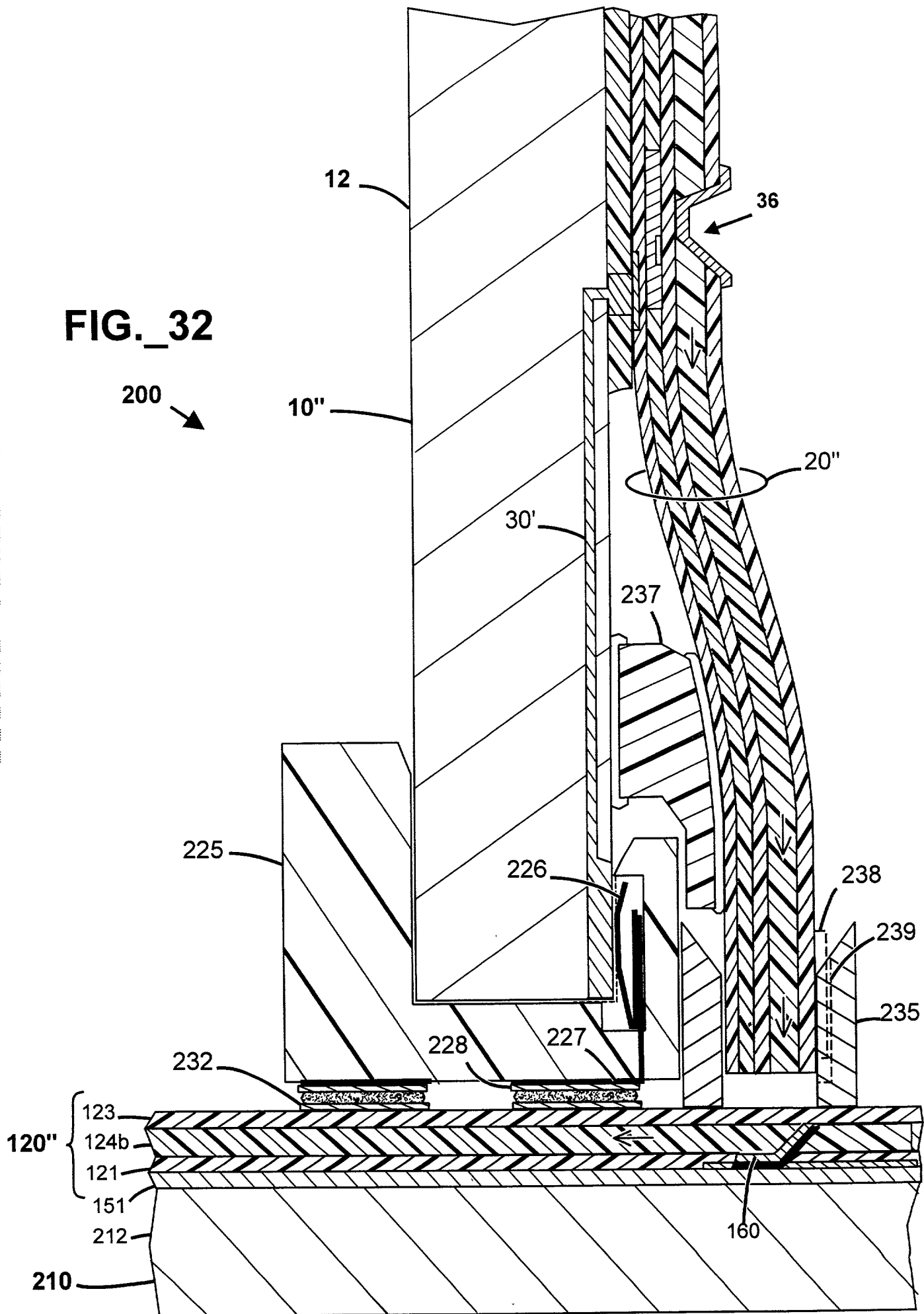
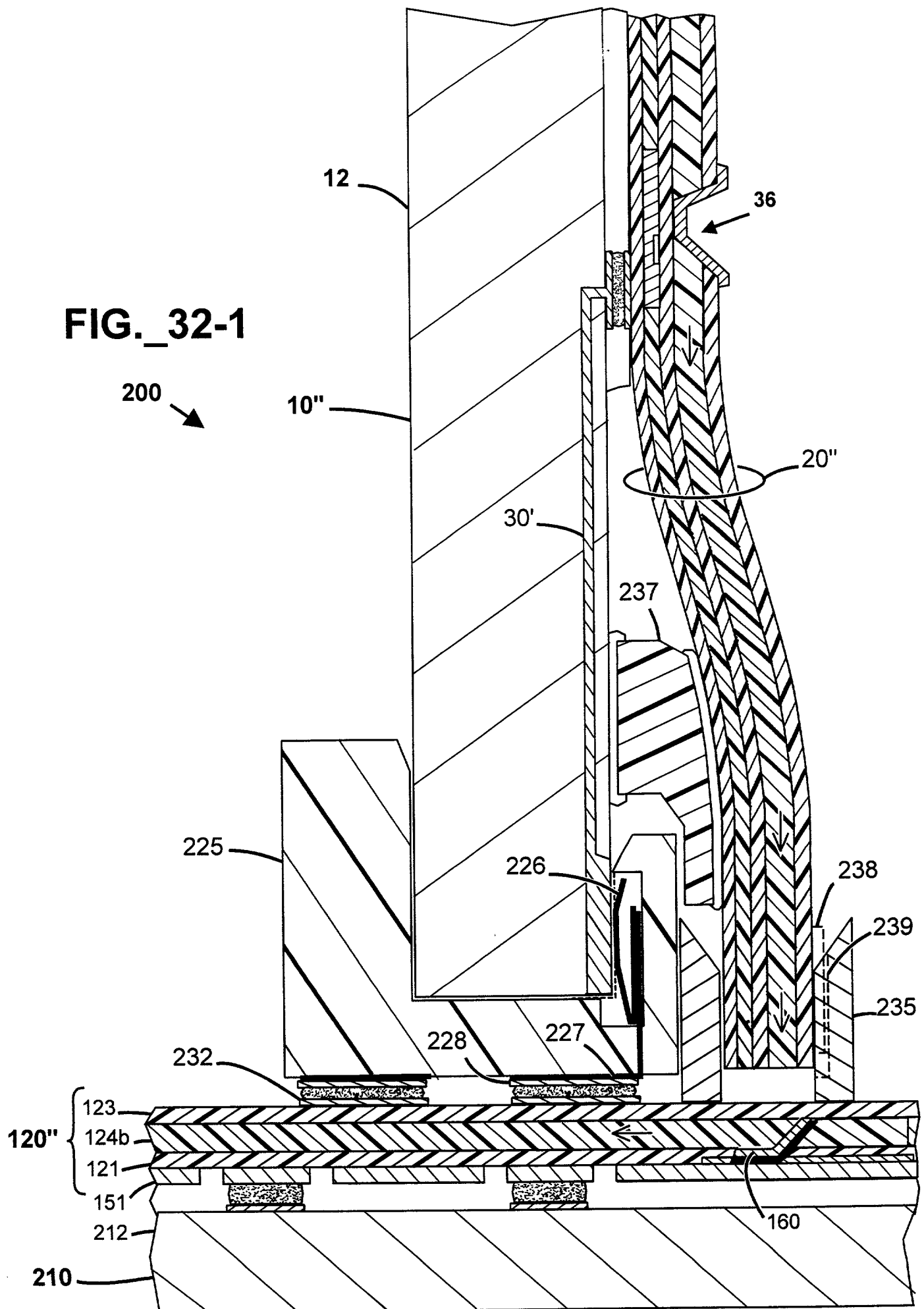
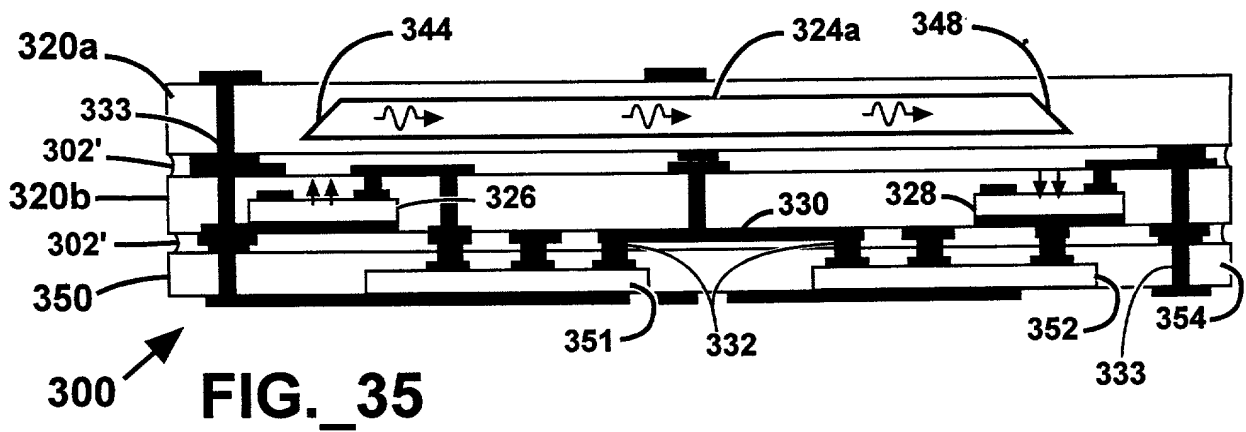
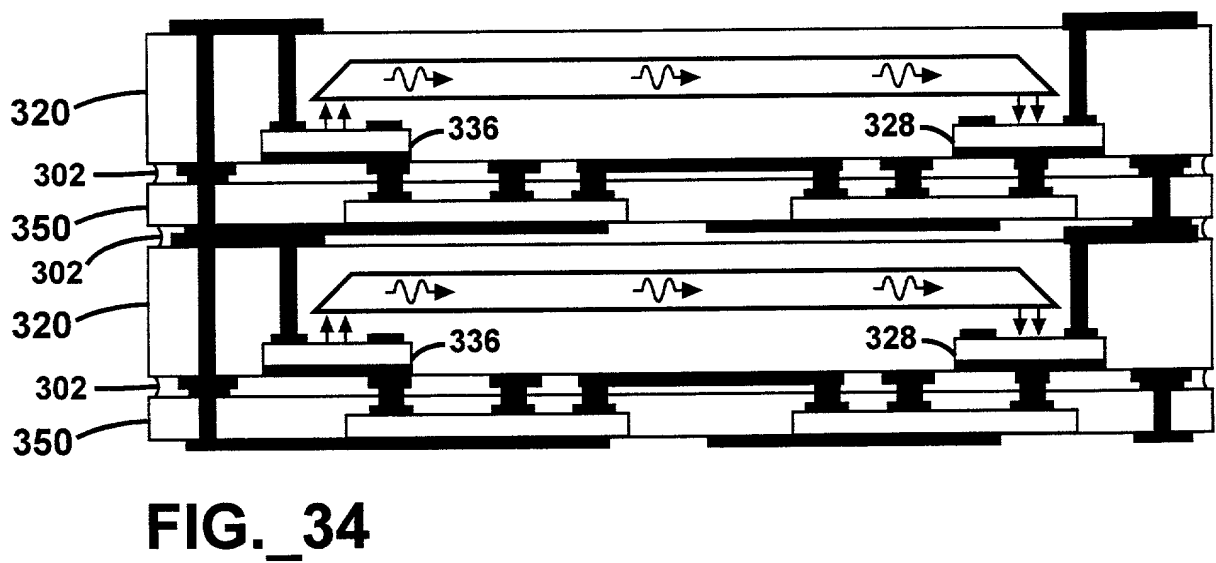
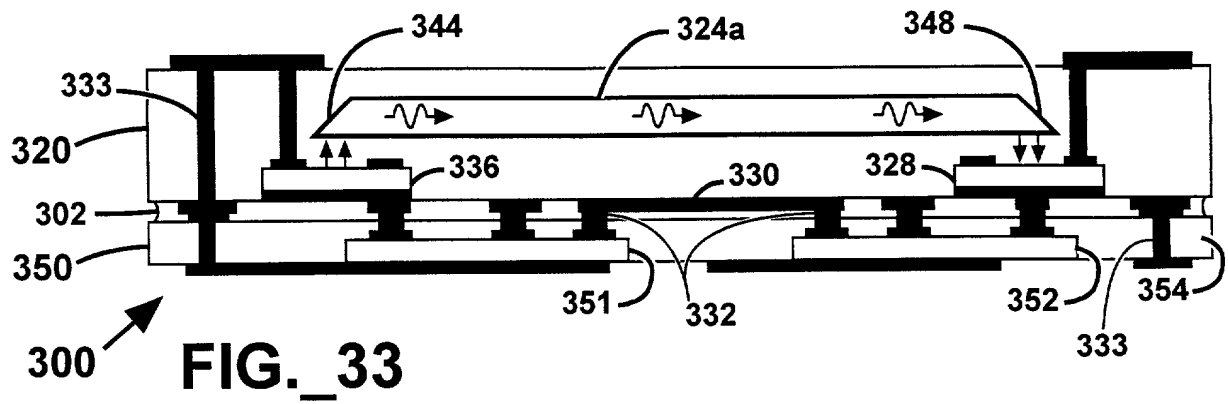


FIG.\_32-1







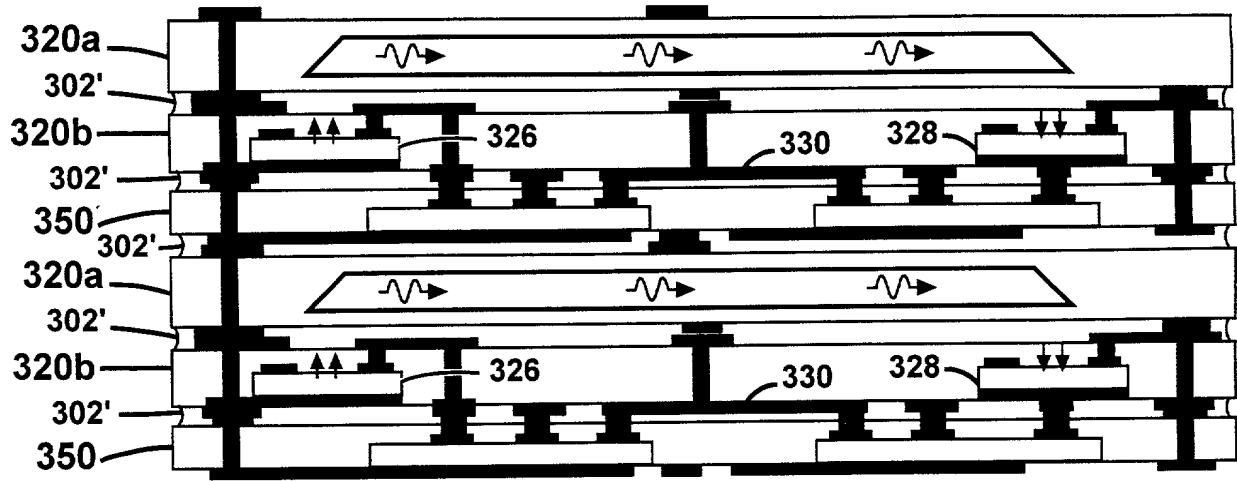


FIG. 36

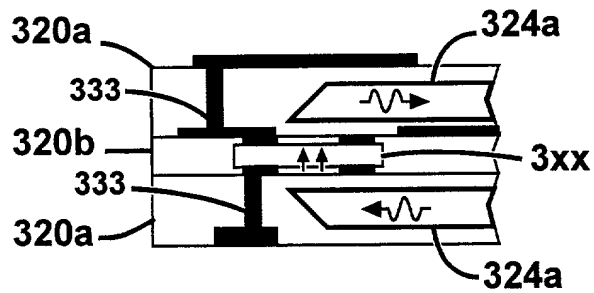


FIG. 37-1

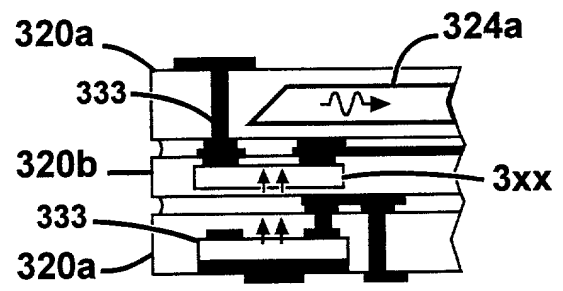


FIG. 37-2

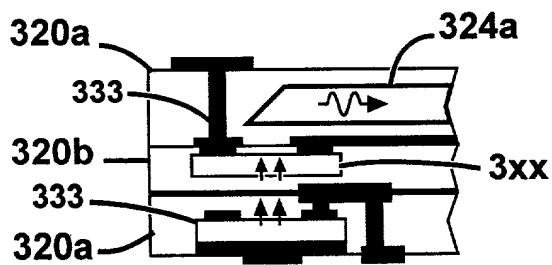


FIG. 37-3

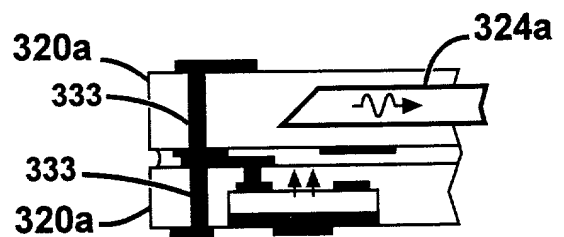
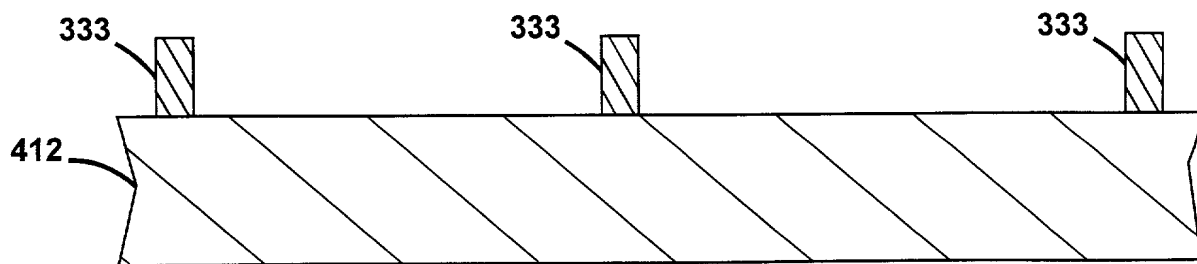
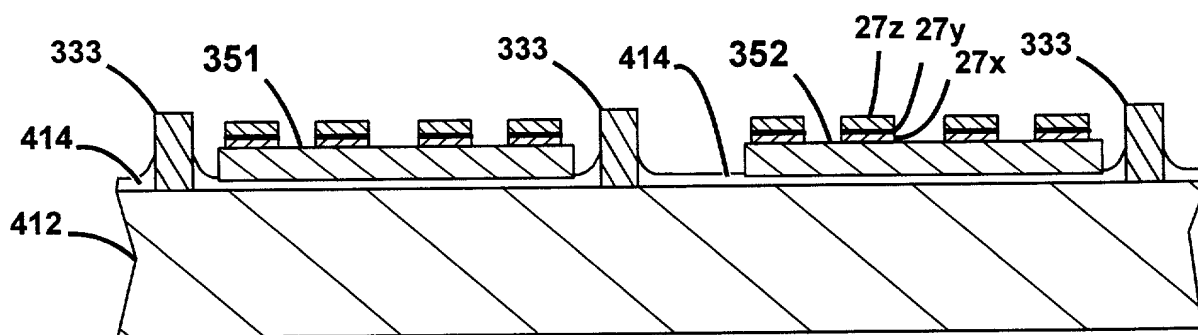


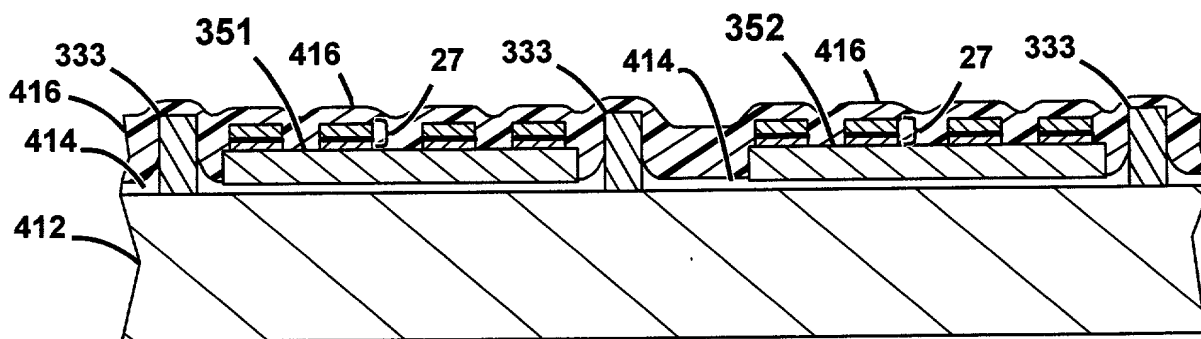
FIG. 37-4



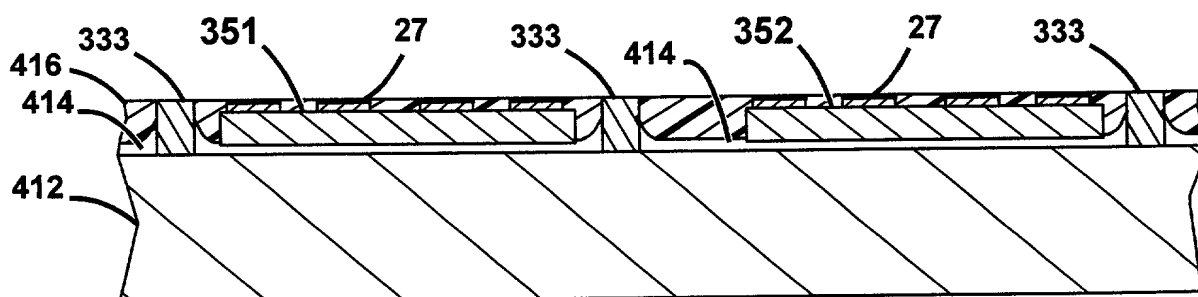
**FIG.\_38**



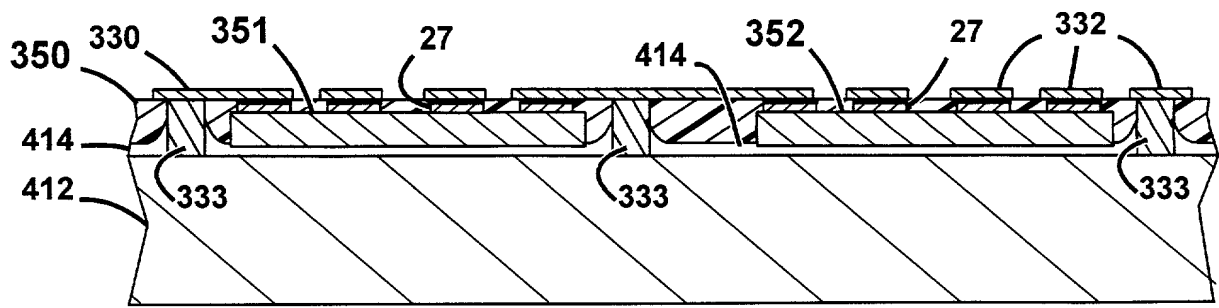
**FIG.\_39**



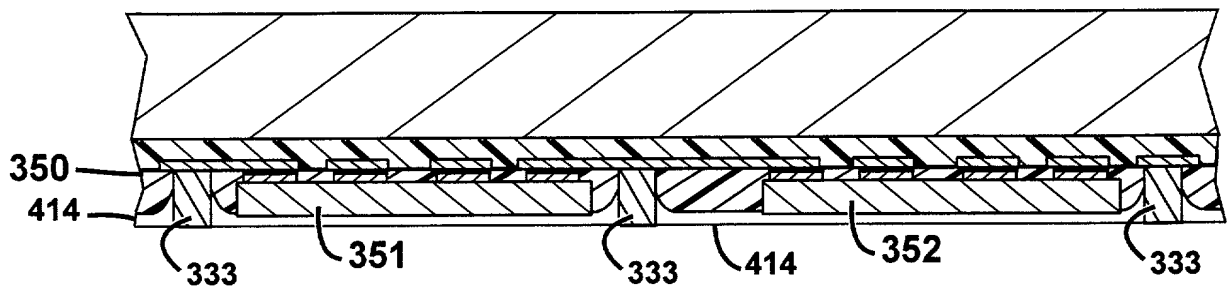
**FIG.\_40**



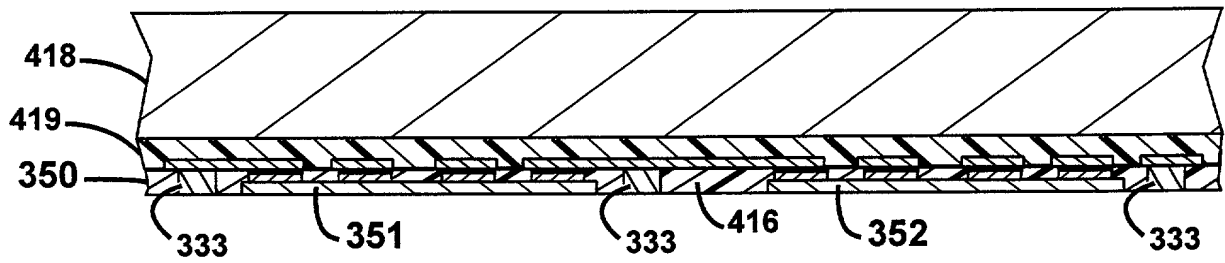
**FIG.\_41**



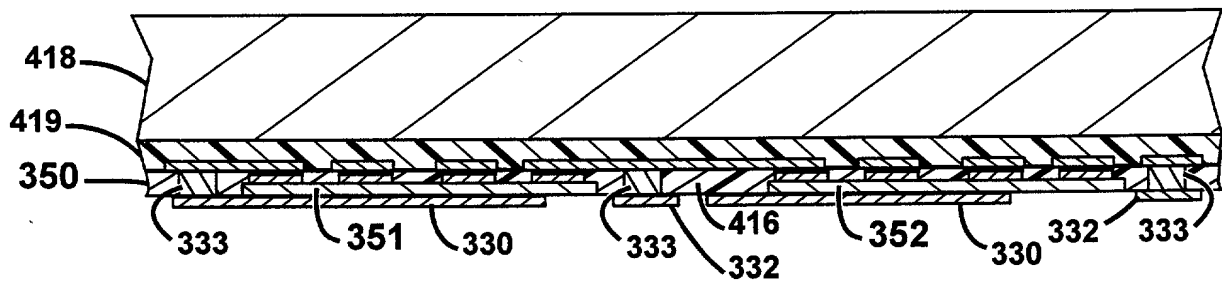
**FIG.\_42**



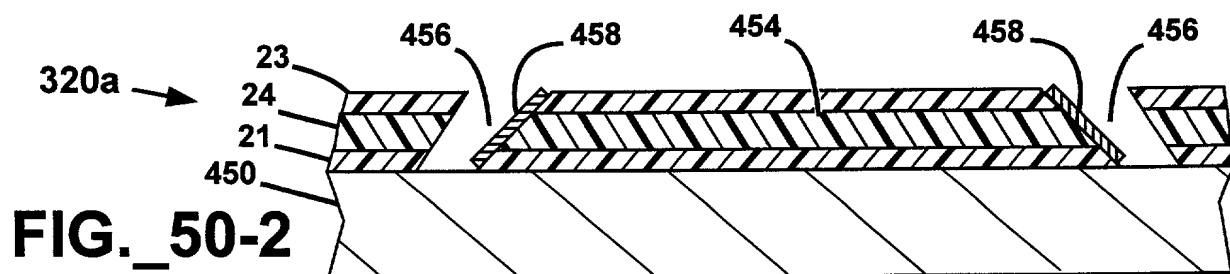
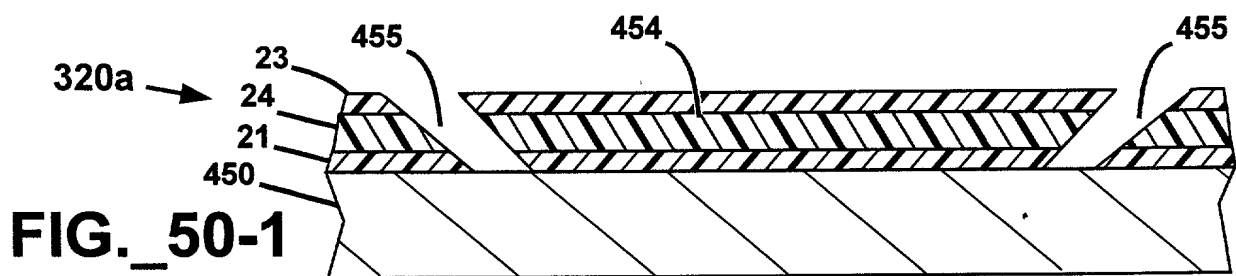
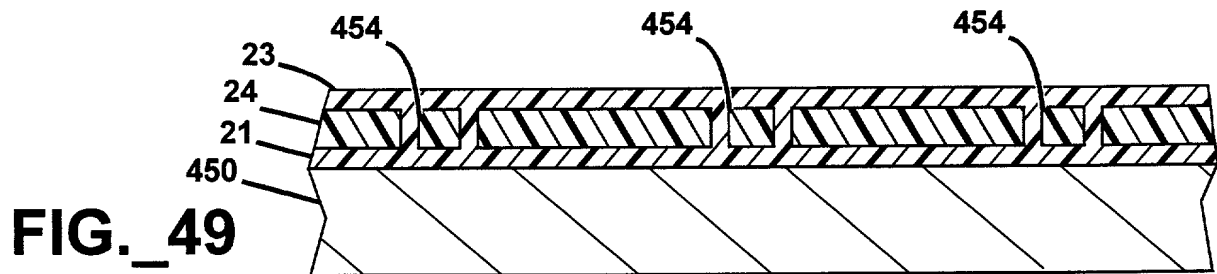
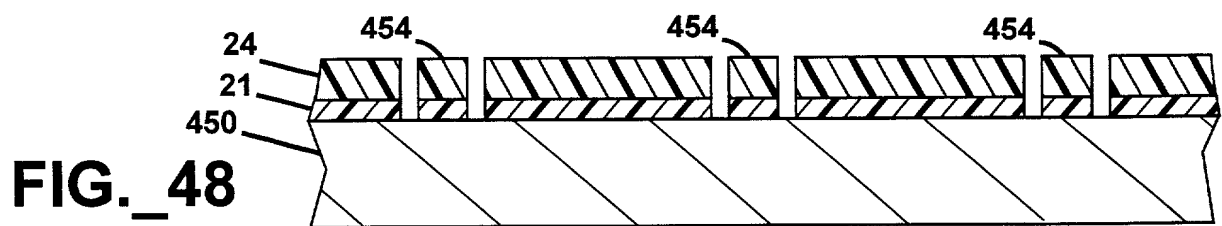
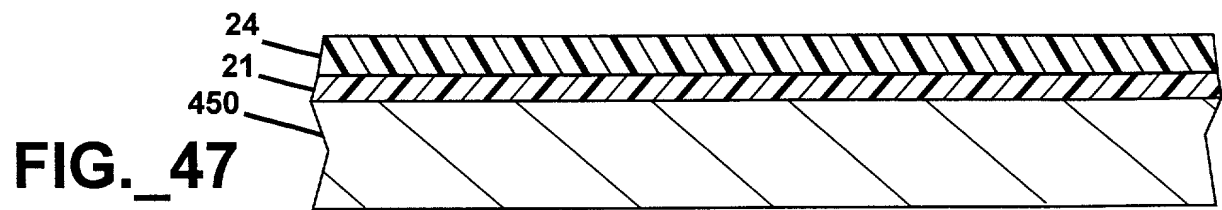
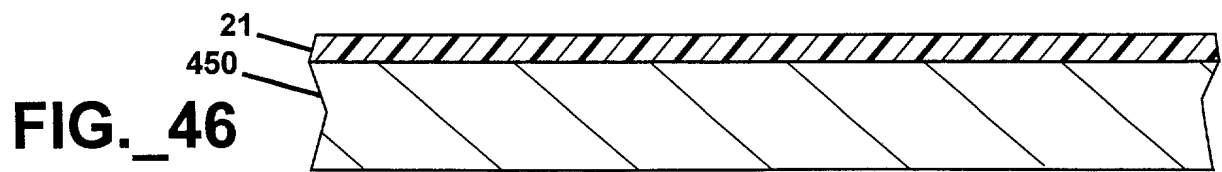
**FIG.\_43**

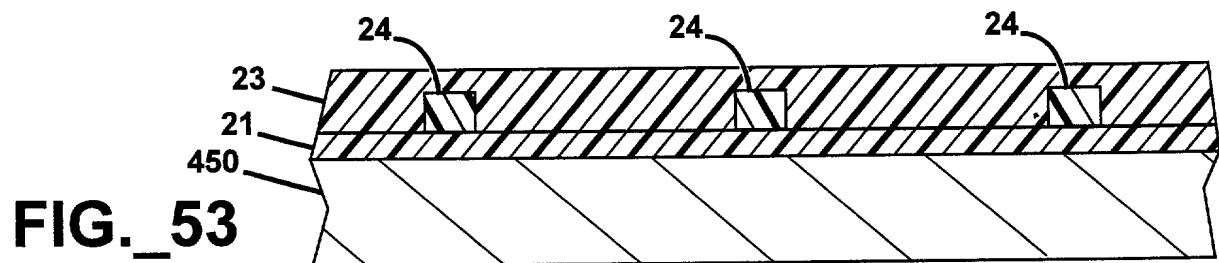
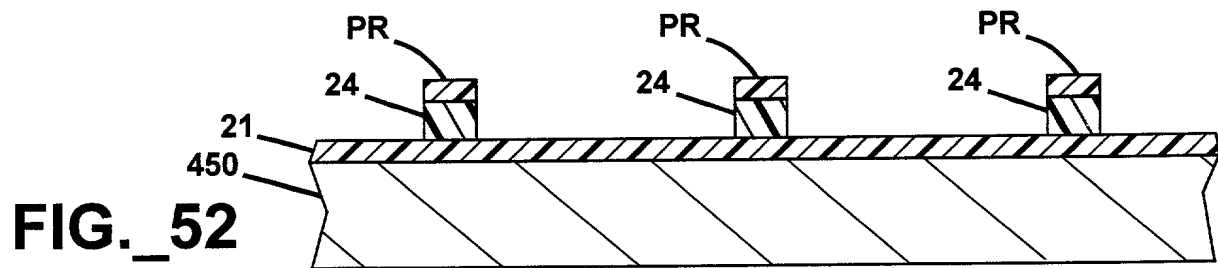
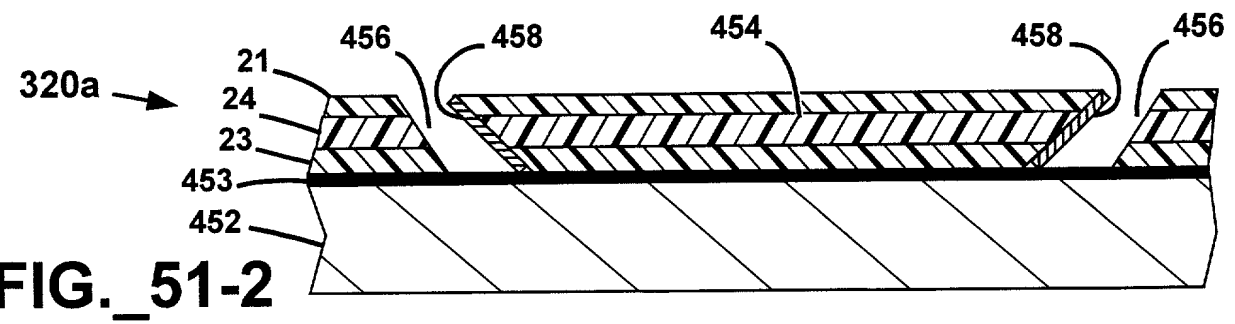
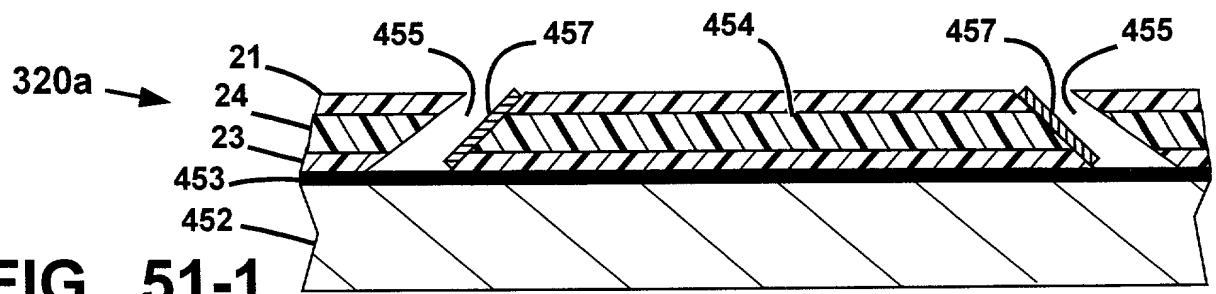


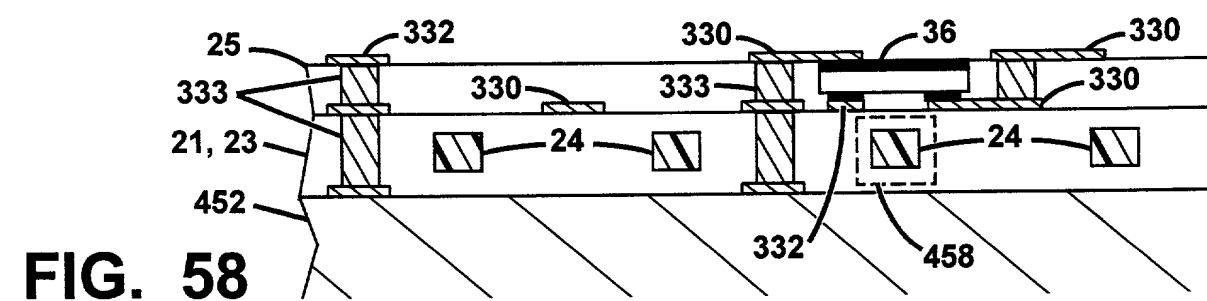
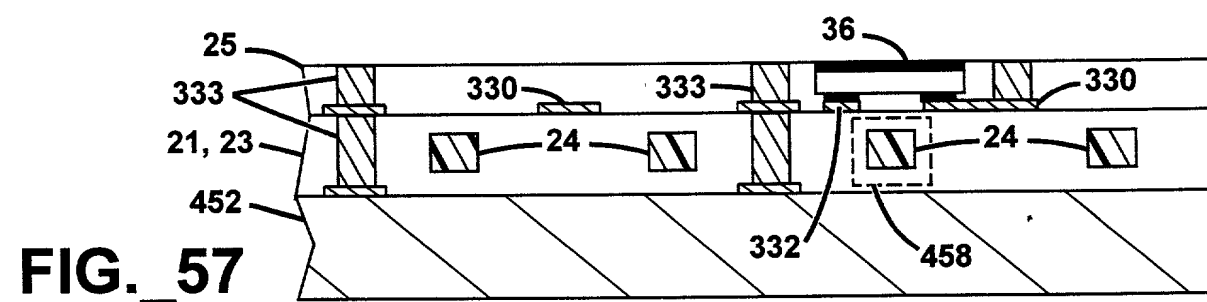
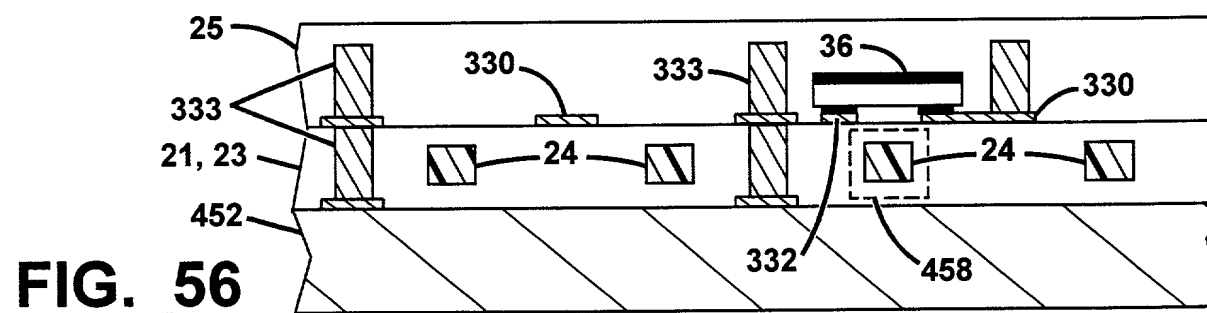
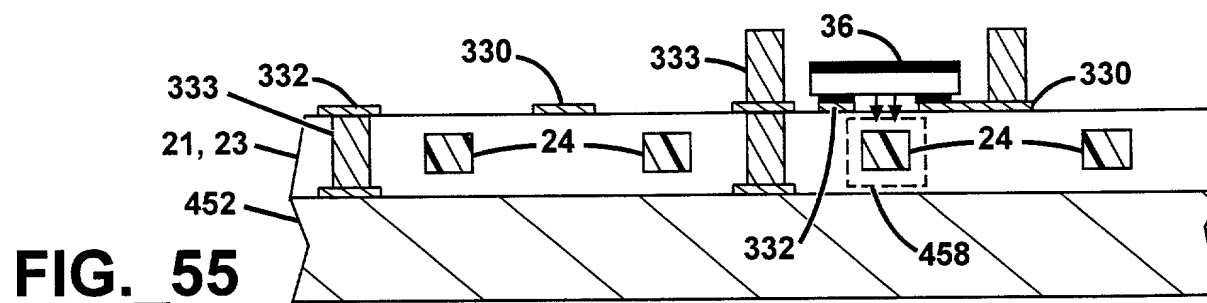
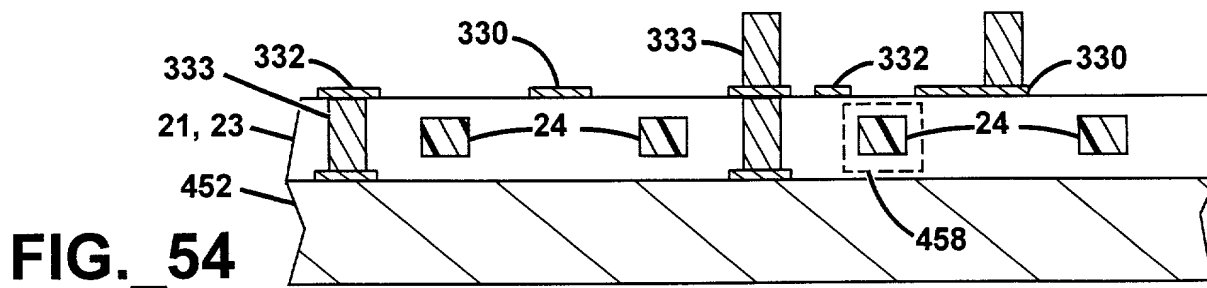
**FIG.\_44**

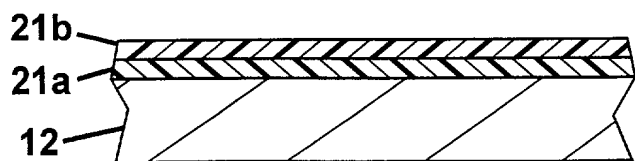


**FIG.\_45**

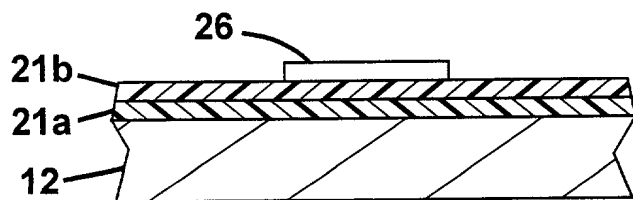




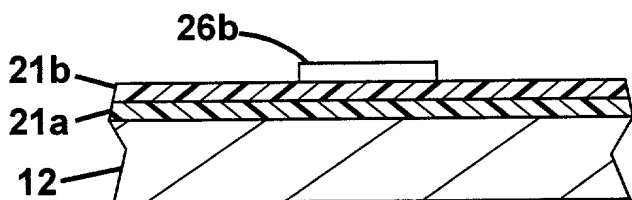




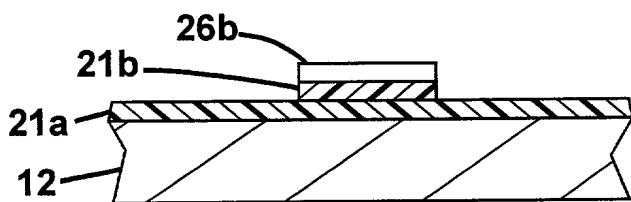
**FIG.\_59**



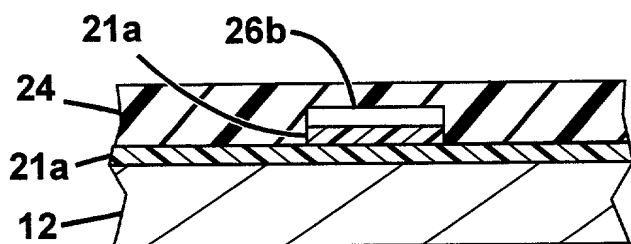
**FIG.\_60**



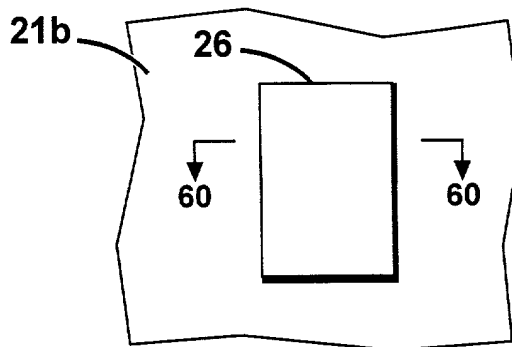
**FIG.\_62**



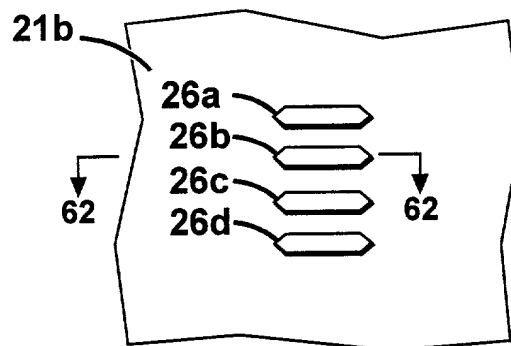
**FIG.\_64**



**FIG.\_65**



**FIG.\_61**



**FIG.\_63**





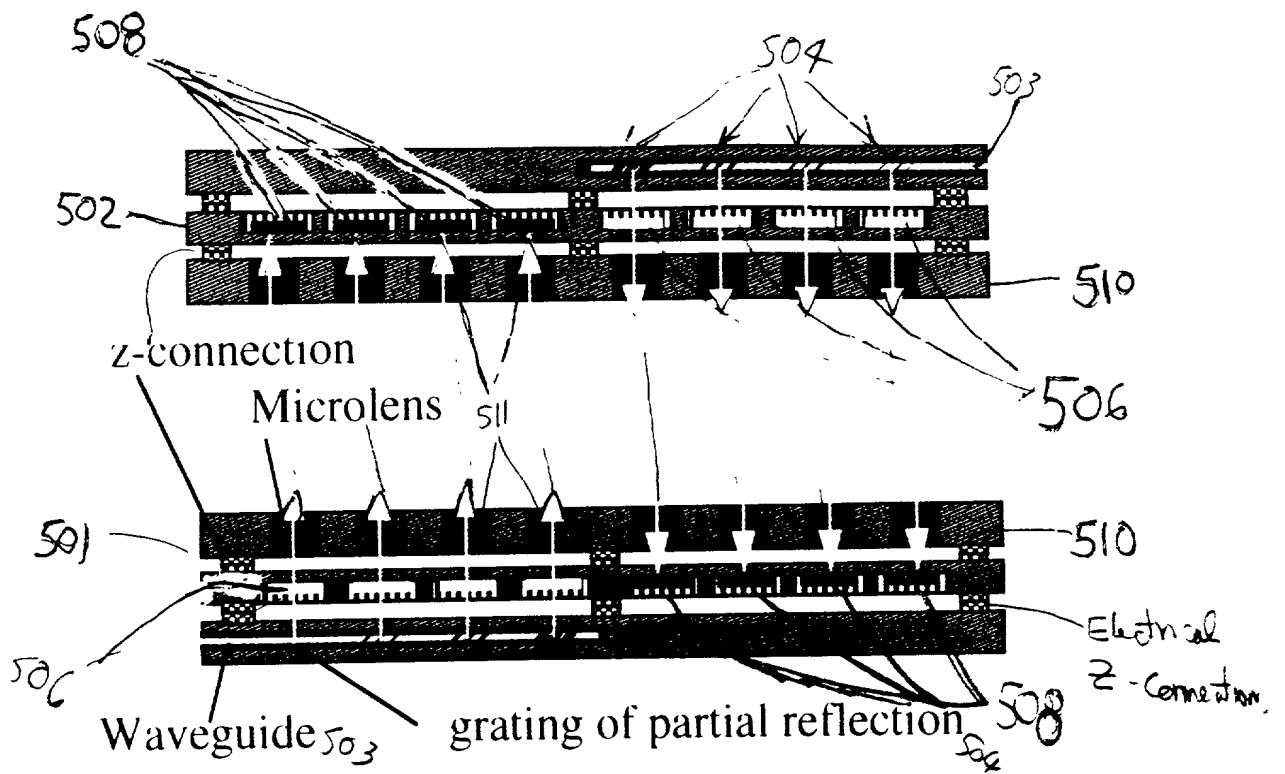


FIG. 69

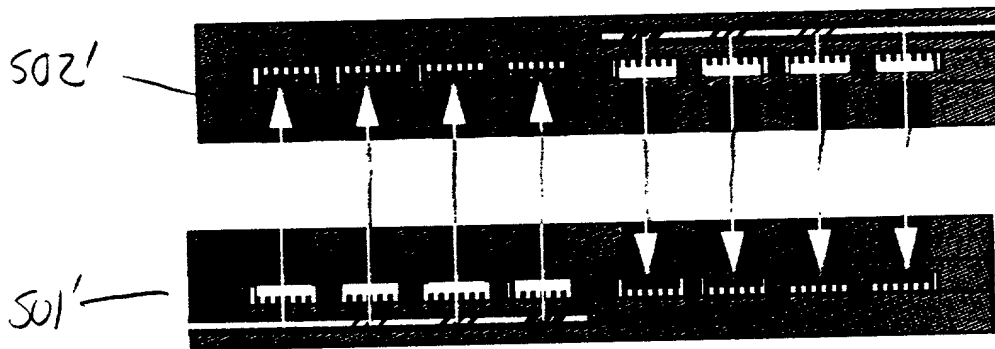


FIG. 70

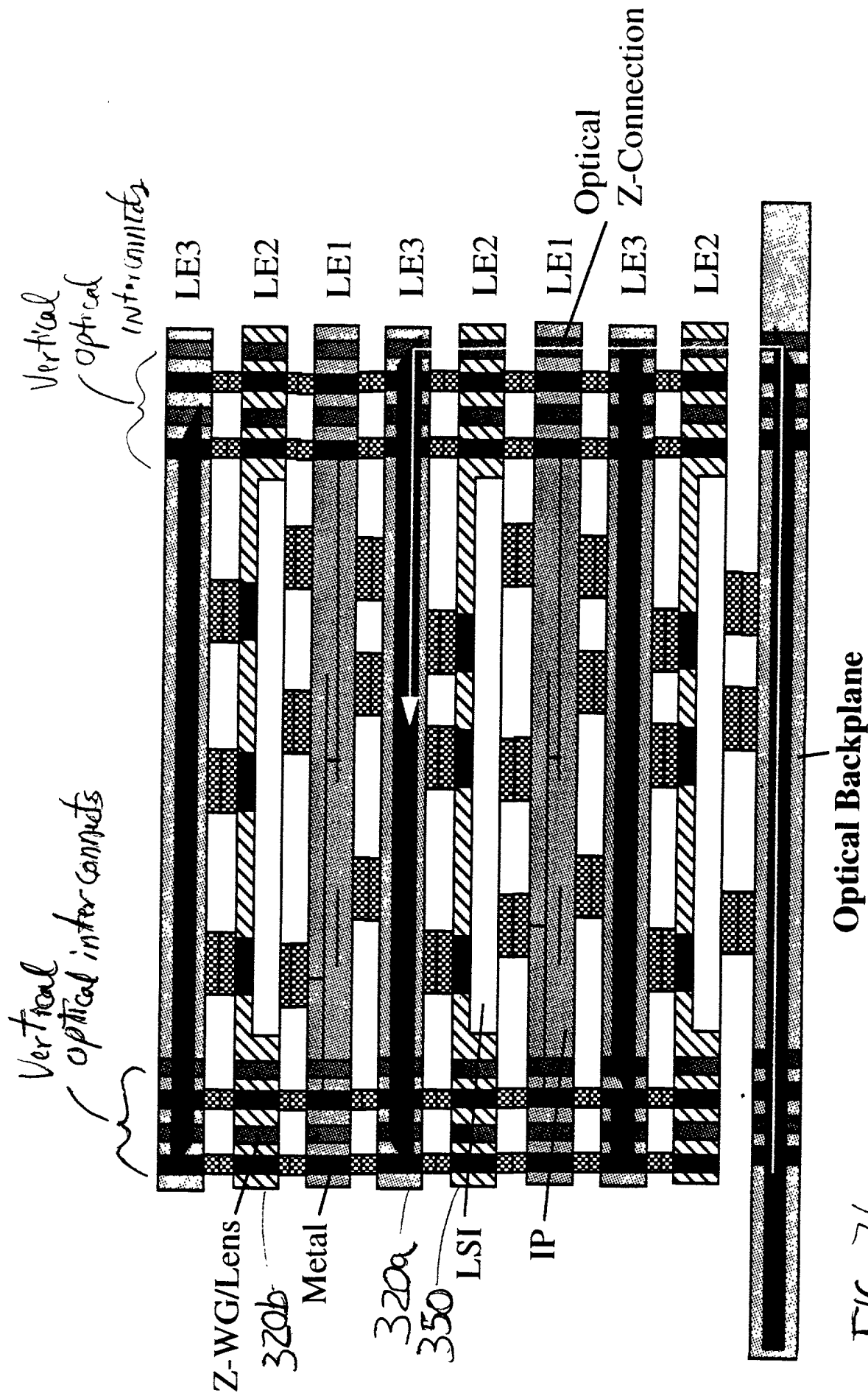
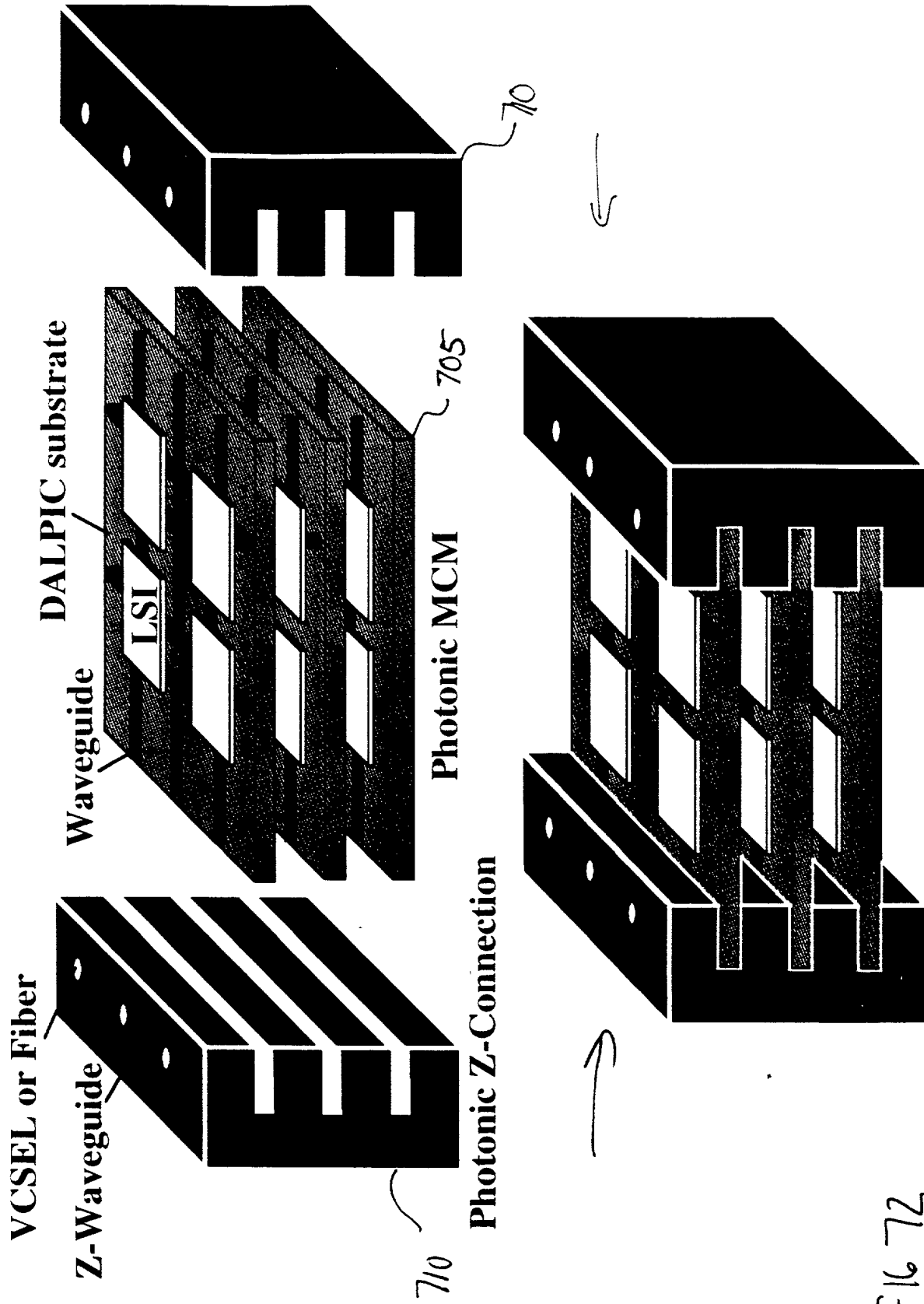


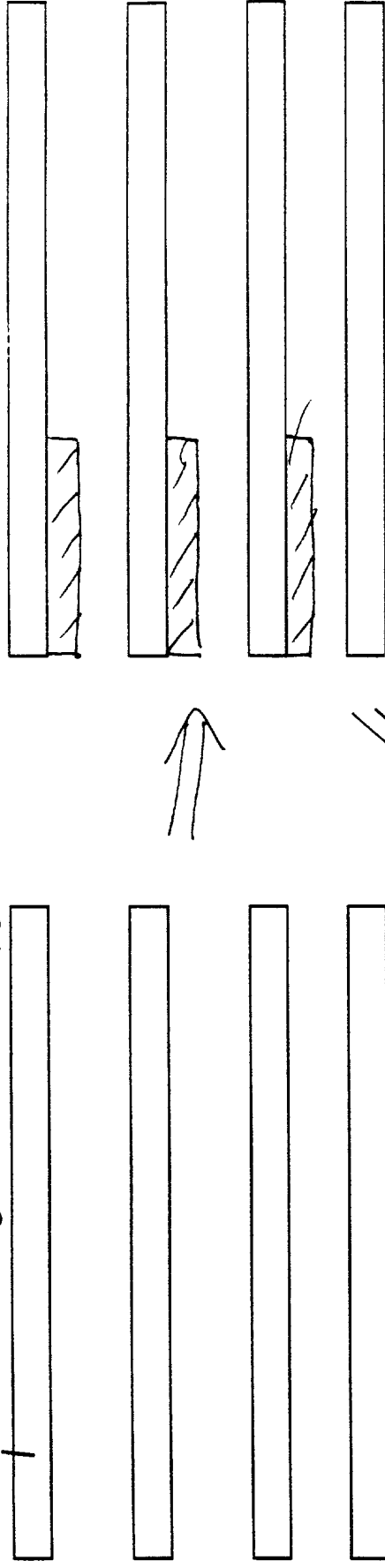
FIG. 71



F1672

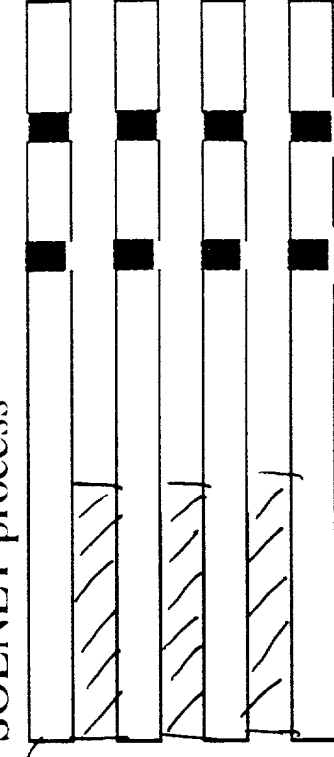
Flexible Photo-imagable sheet (Polyguide)

Bonding sheet attach

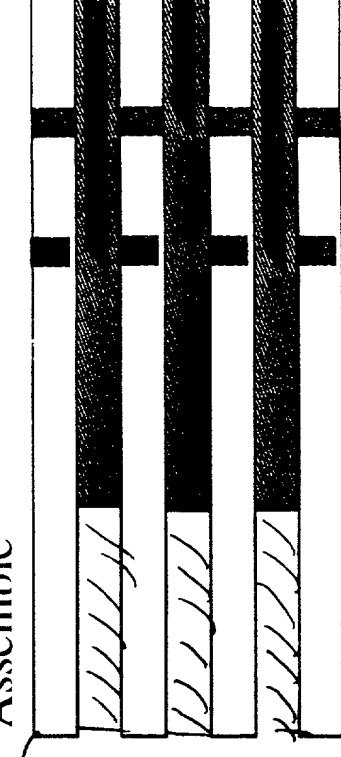


Exposure

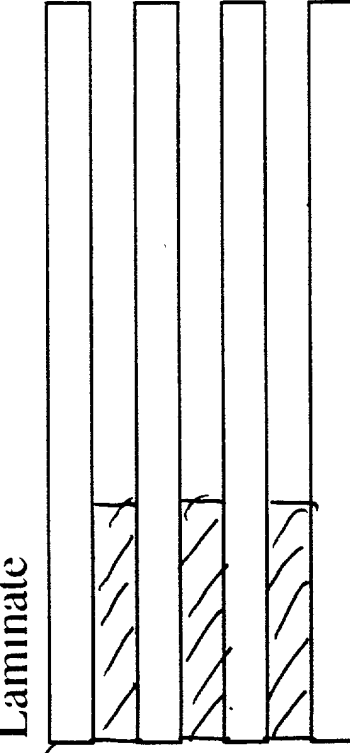
SOLNET process



Assemble



Laminate



Post cure

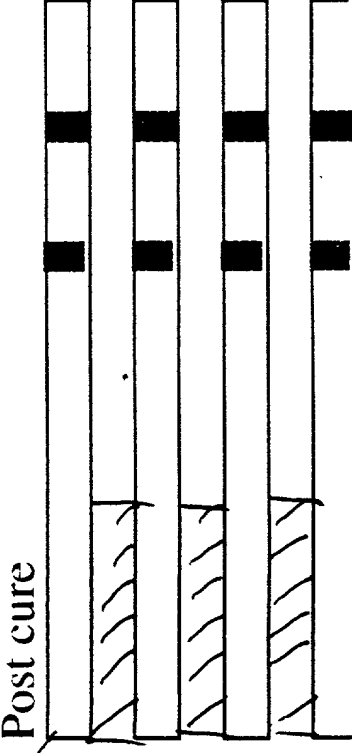
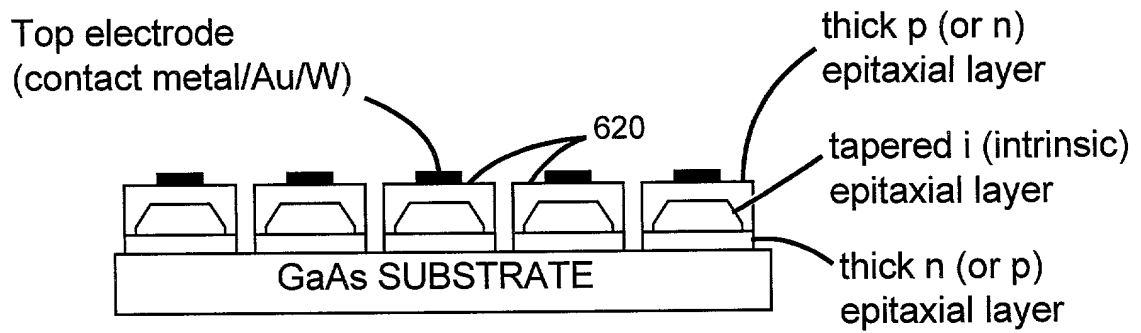
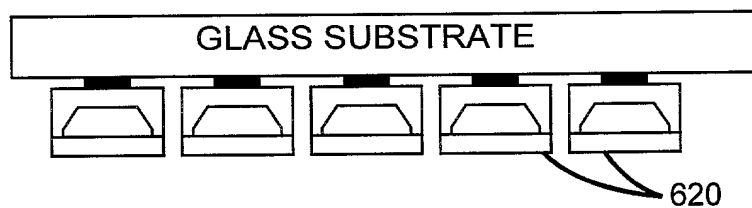


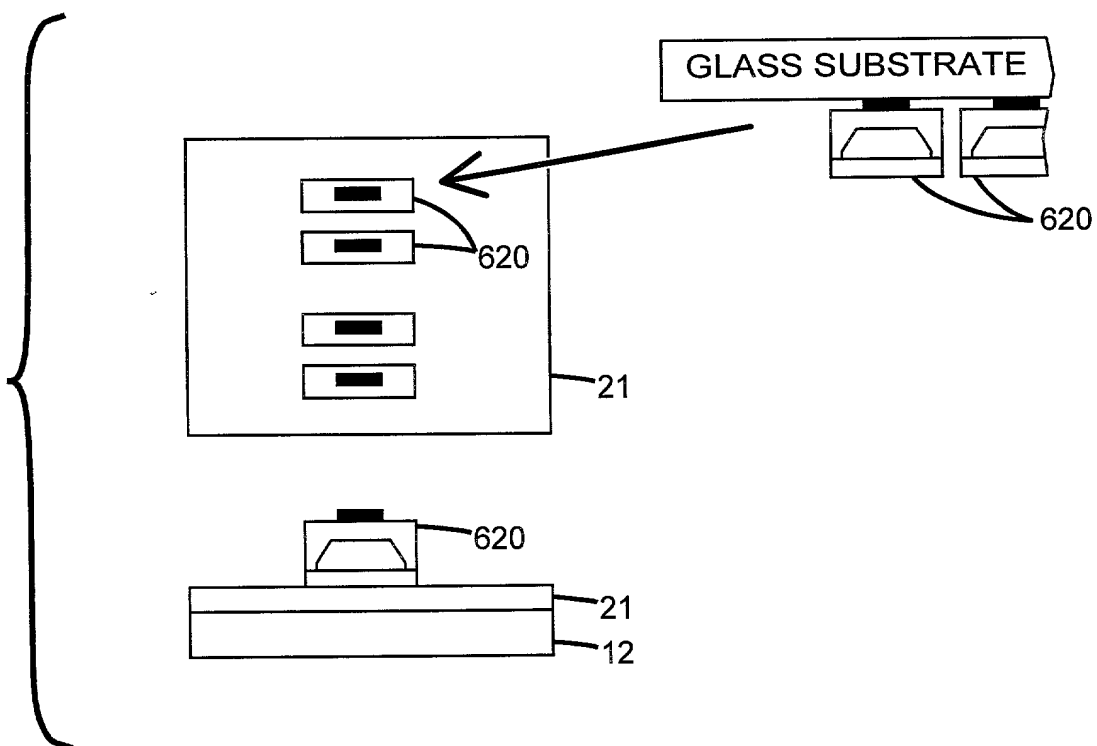
FIG. 73



**FIG.\_74** (Epitaxial growth and patterning)



**FIG.\_75** (Epitaxial liftoff)



**FIG.\_76** (Transfer)

# Example of Light Modulator (or Photodetector) Integration

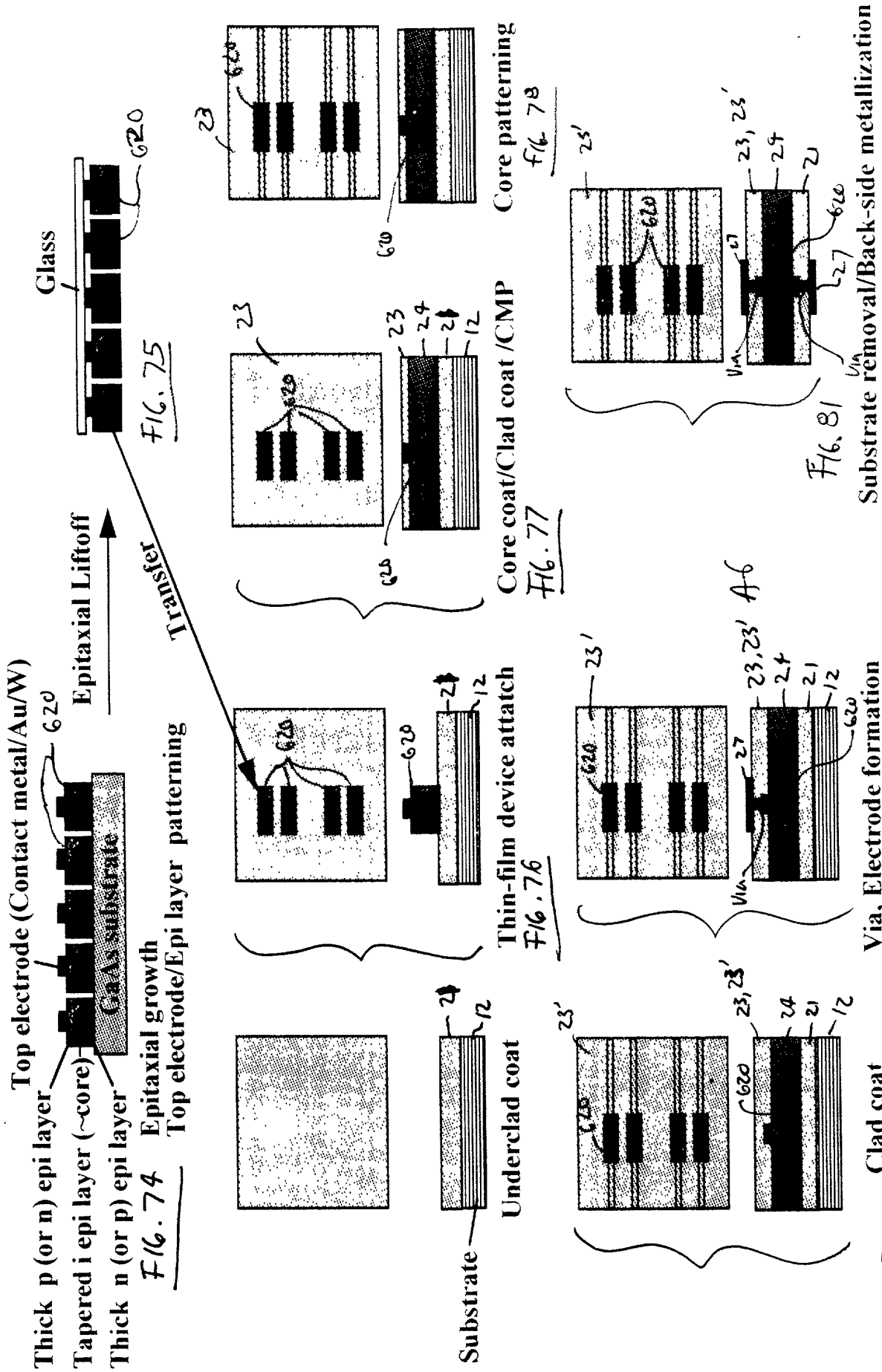


Fig. A6

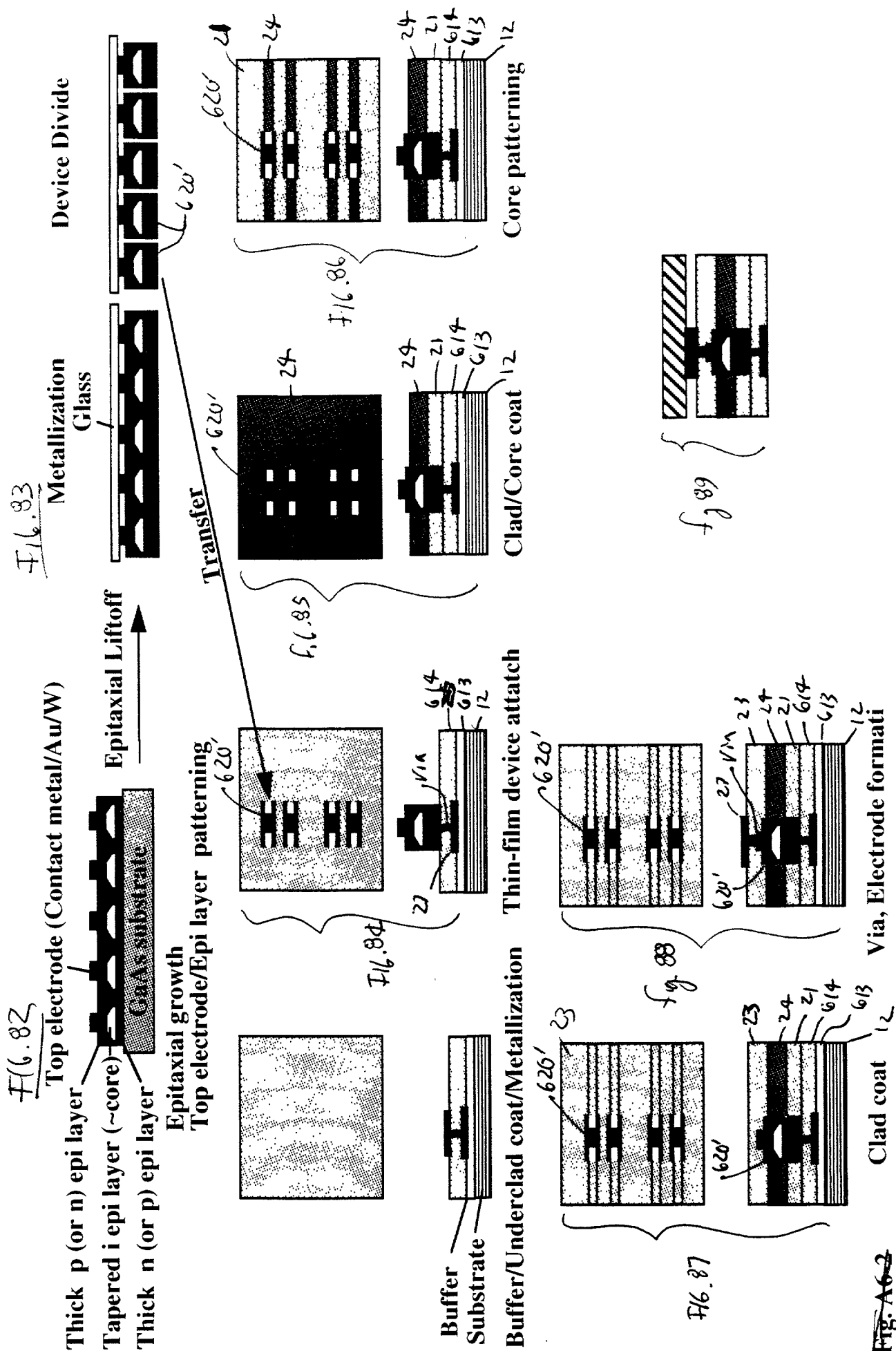
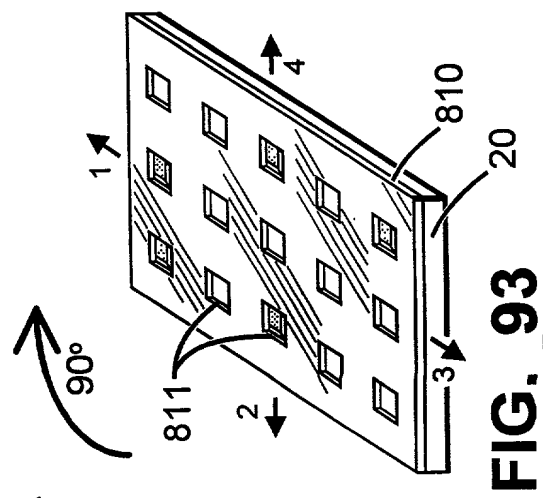
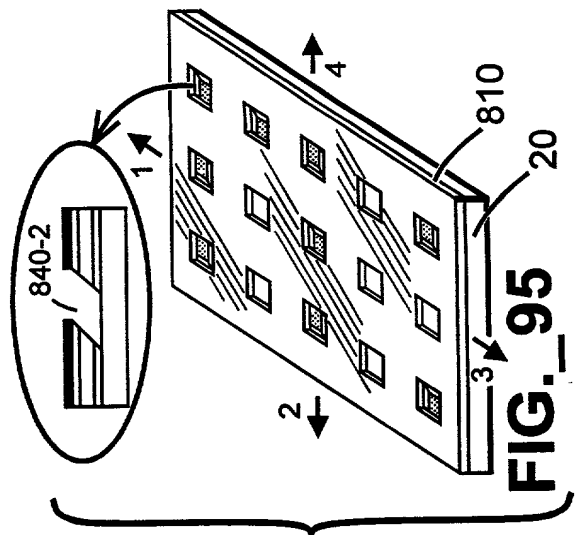
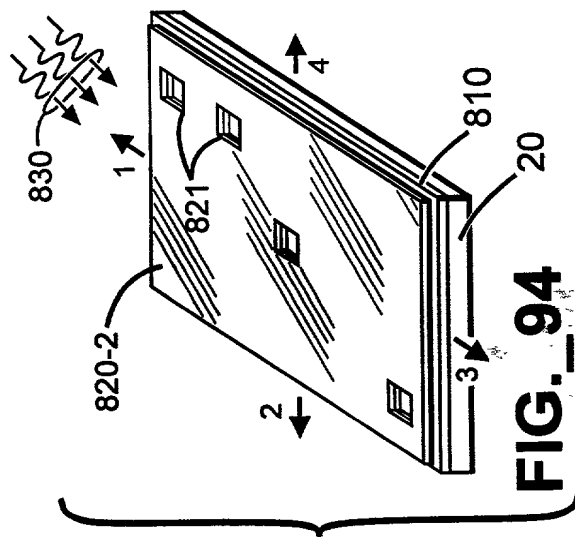
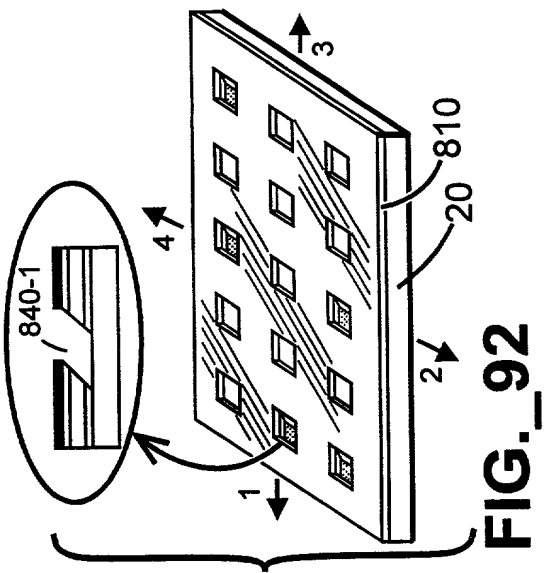
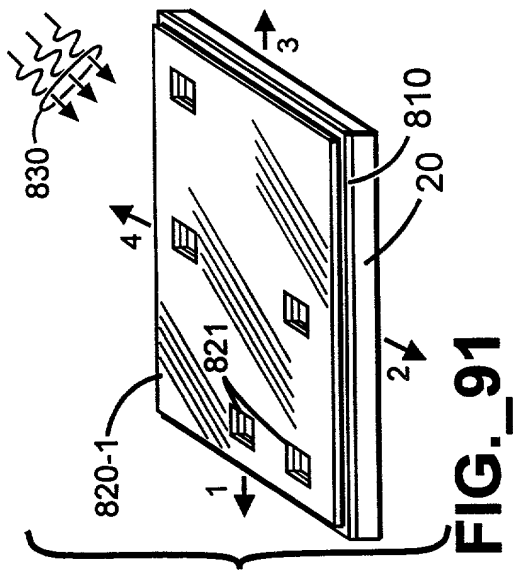
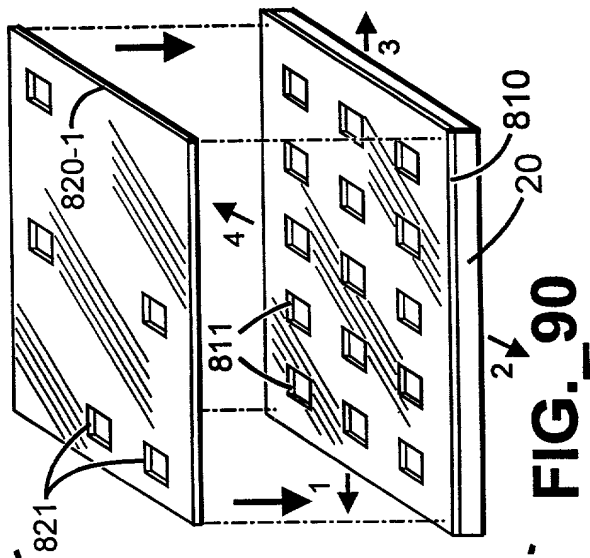


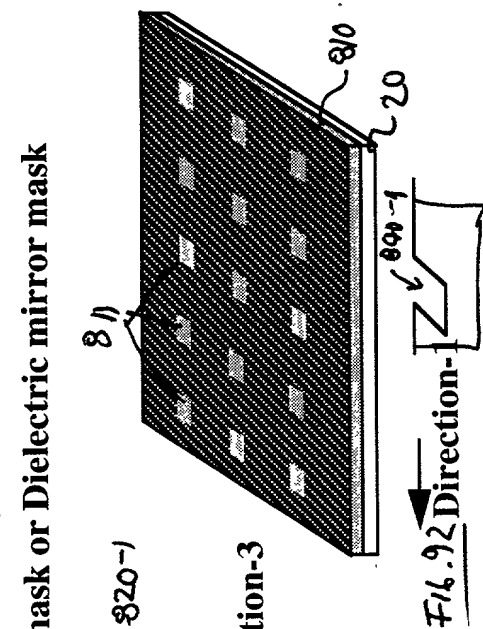
Fig. A62



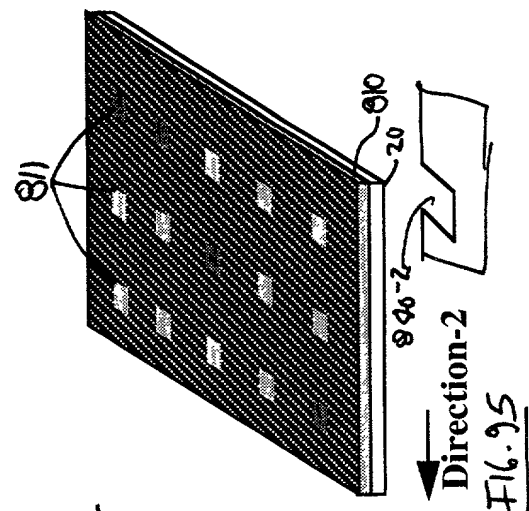
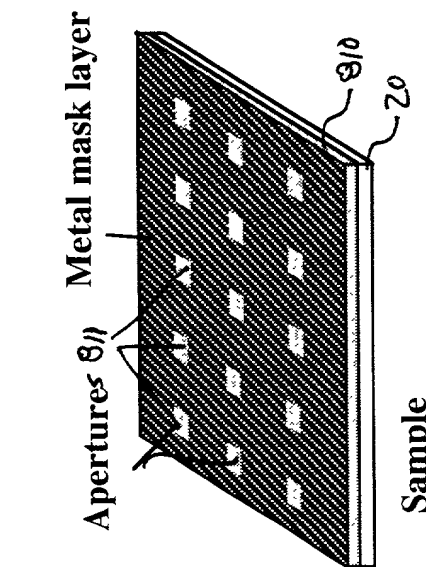
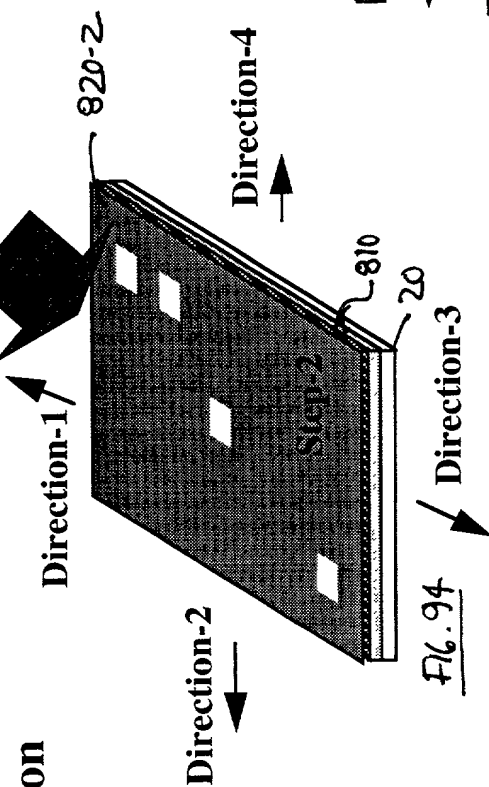


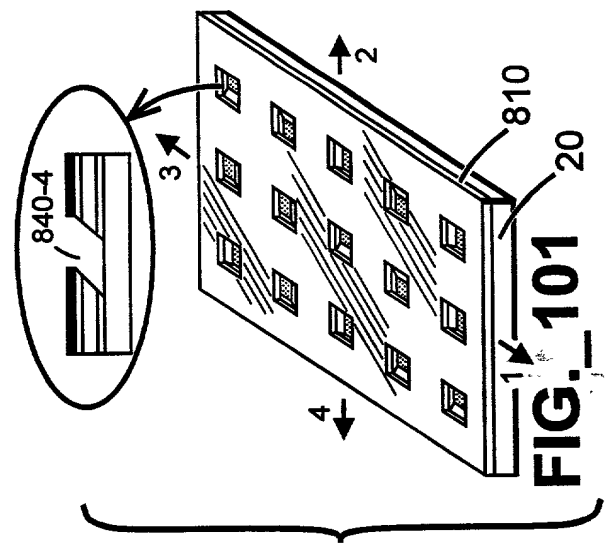
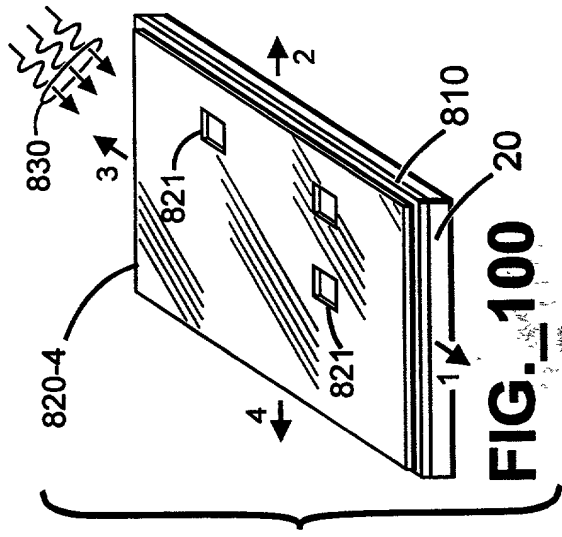
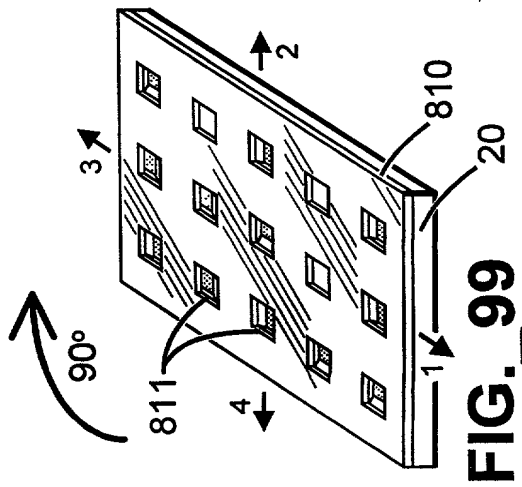
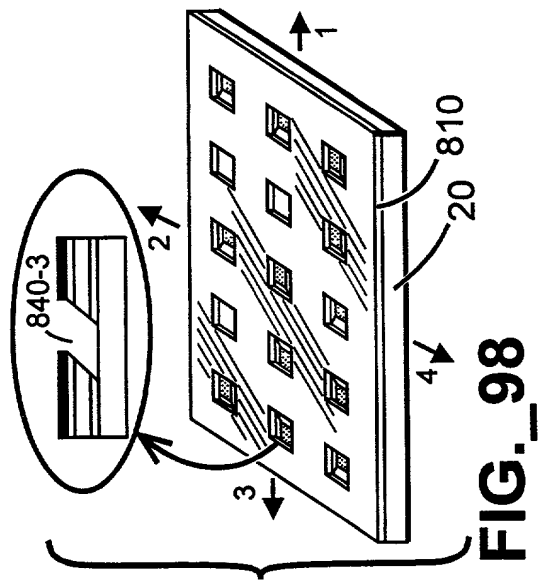
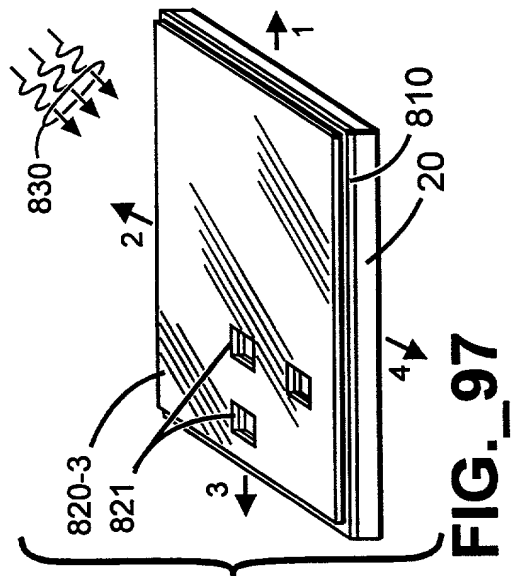
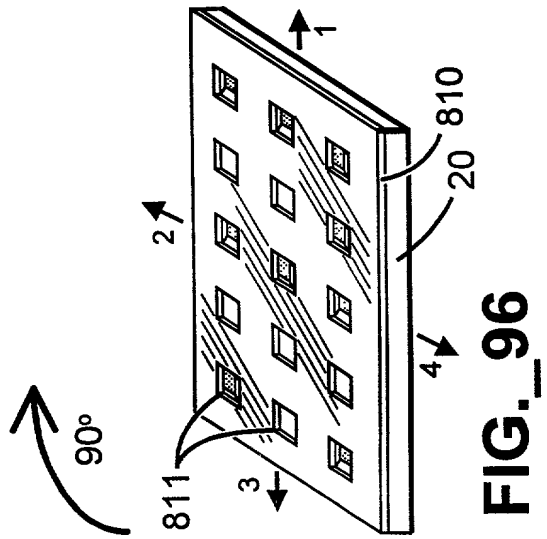
1

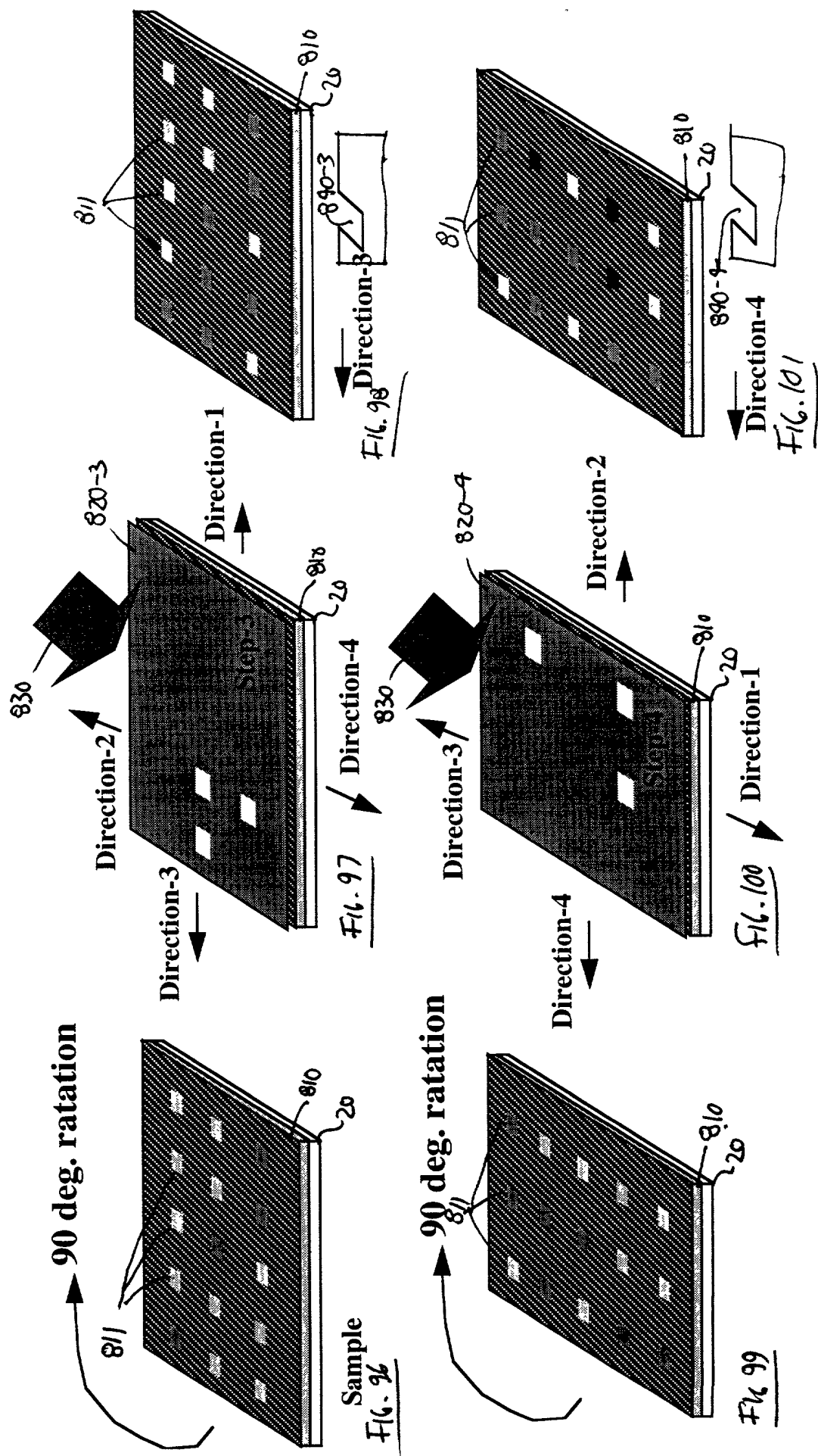
Excimer laser with tilted incident angle

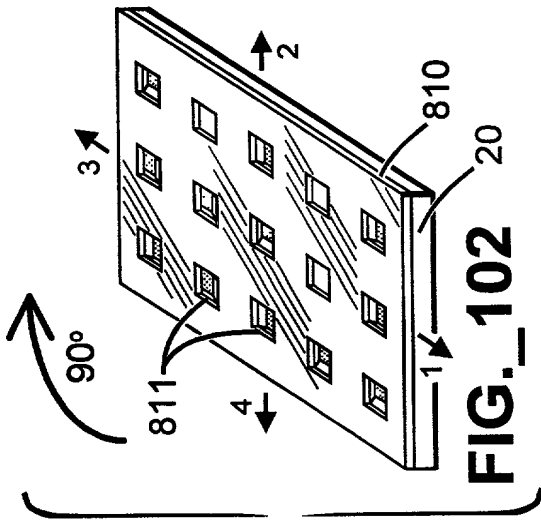
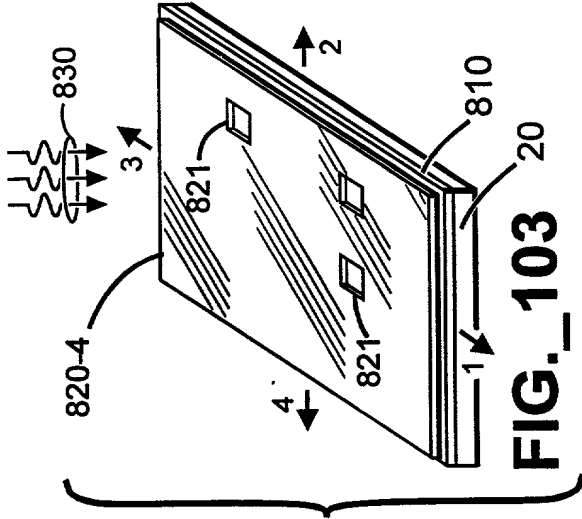
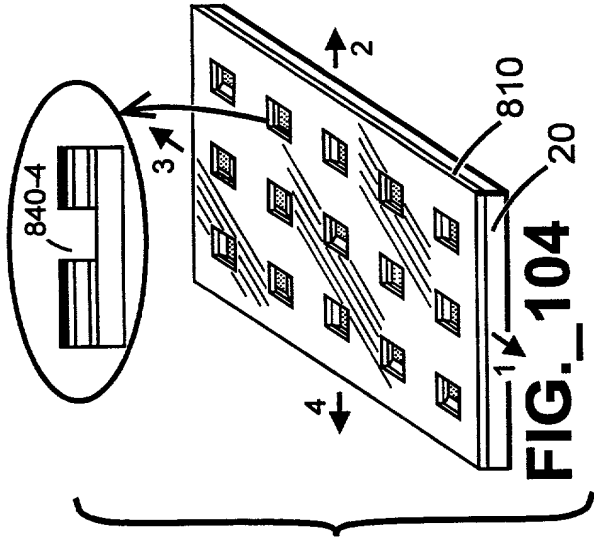


90 deg. rotation









90 deg. rotation

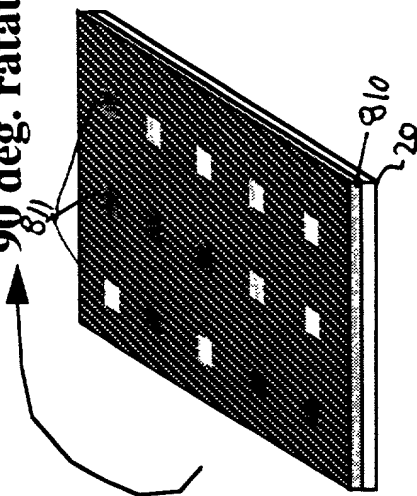


FIG. 102

Direction-4

Direction-2

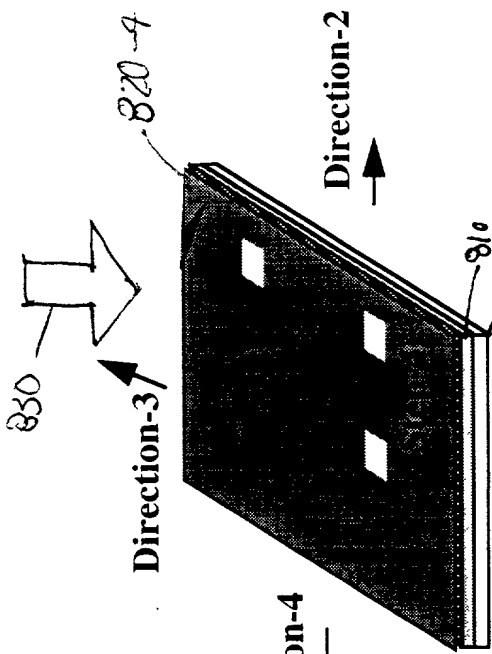


FIG. 103

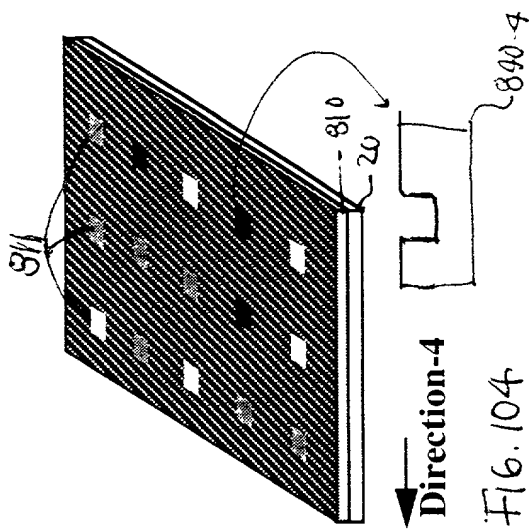


FIG. 104

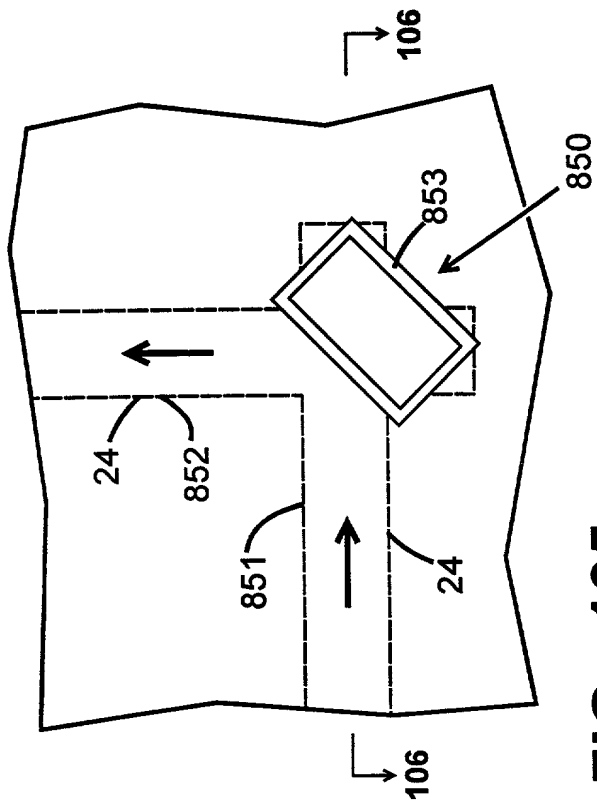


FIG. 105

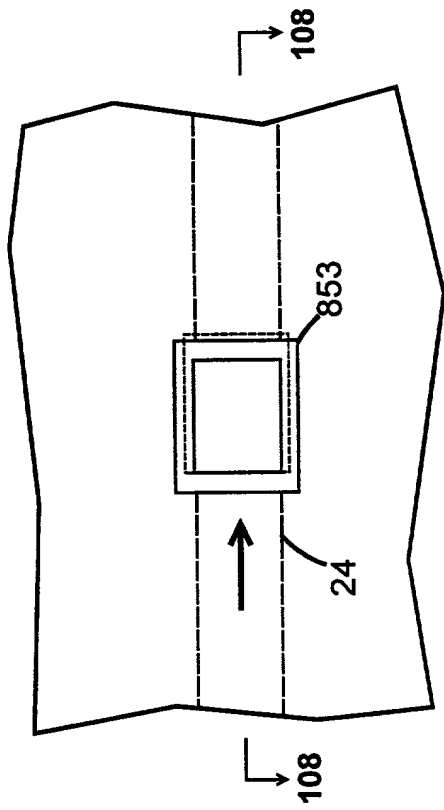


FIG. 107

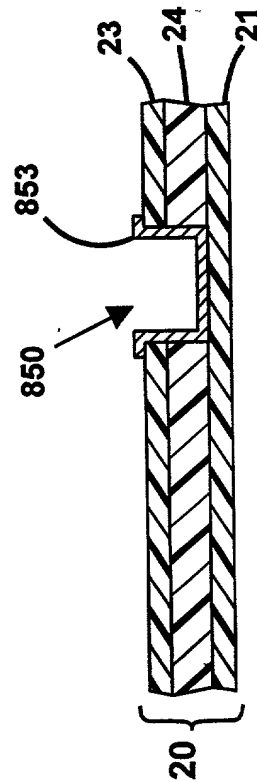


FIG. 106

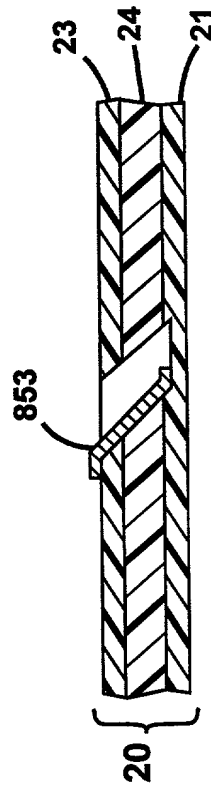


FIG. 108

550240" T6456260

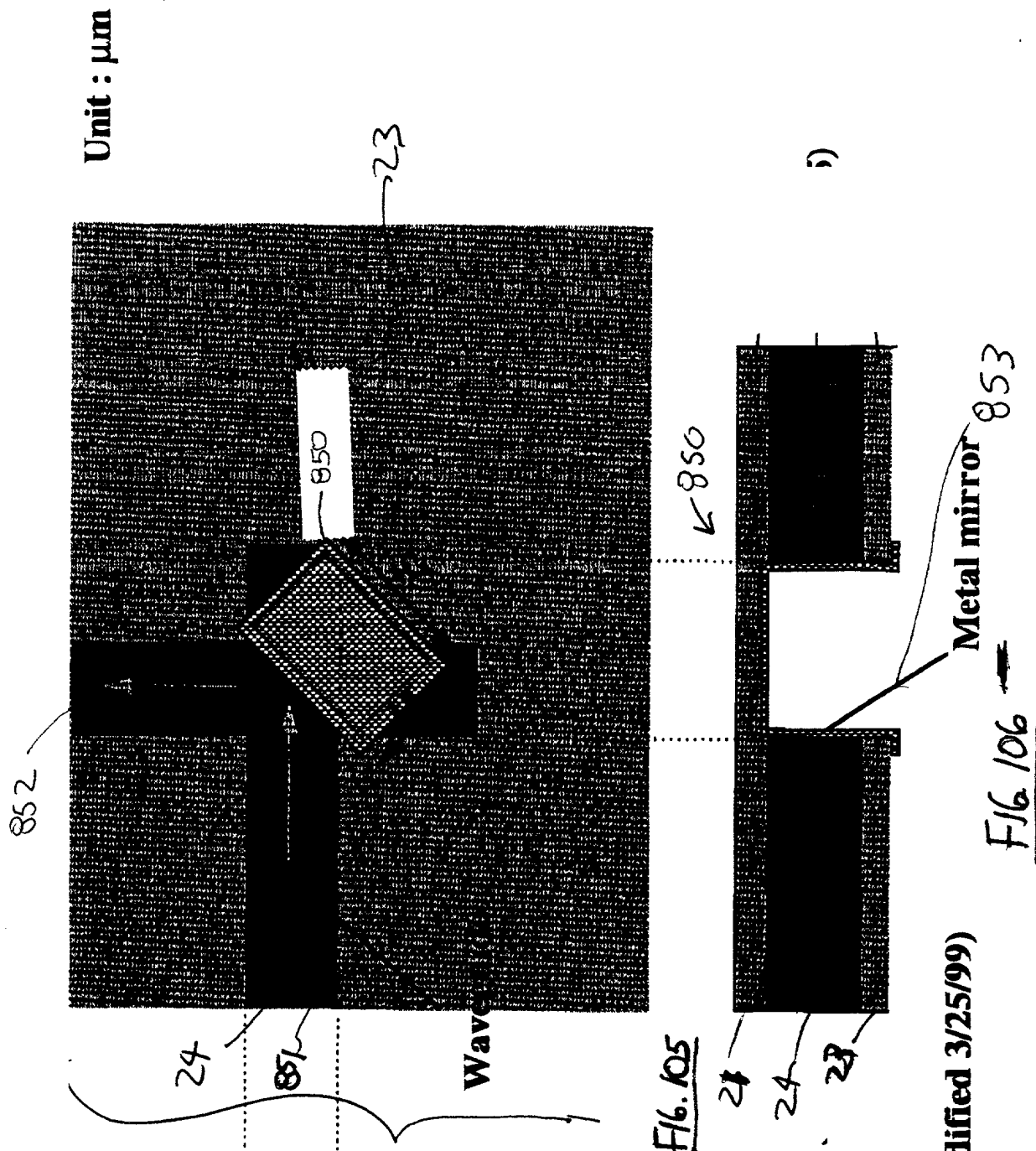


Fig. 3/24/99-1 (Modified 3/25/99)

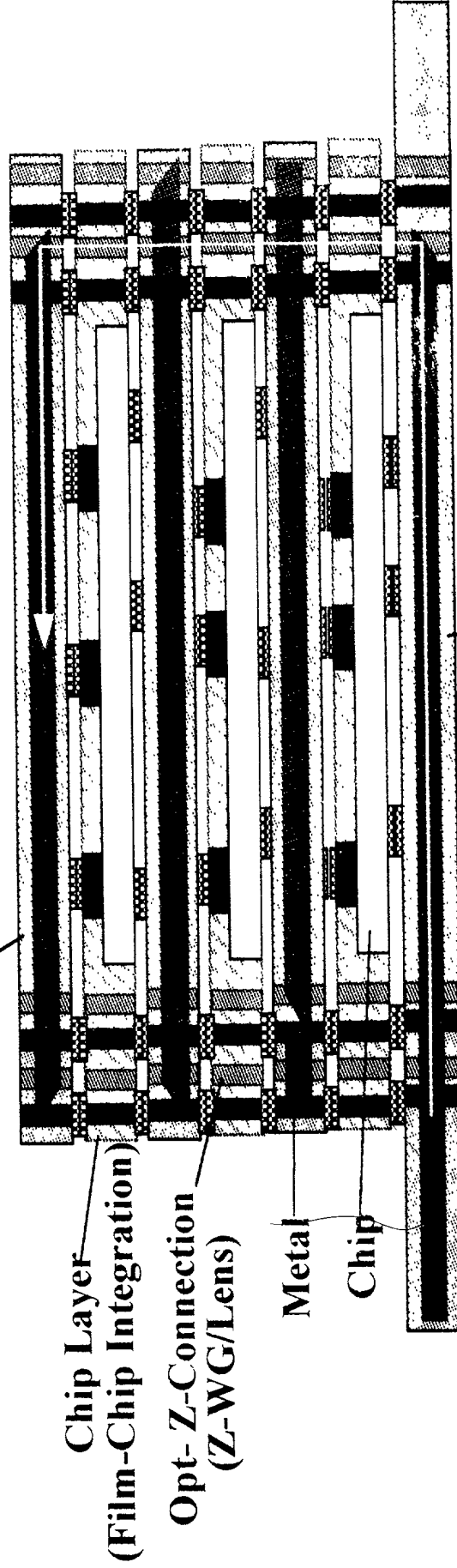
cl 3/25/99





GS CX/CXX OE Solution --- OE-3D-Stack

OE-film-DW (V) or (M)



OE-film-W

A 22

FIG. 109

2/23/99-added 7

Figure 12-1

A 22 3/7/99

122

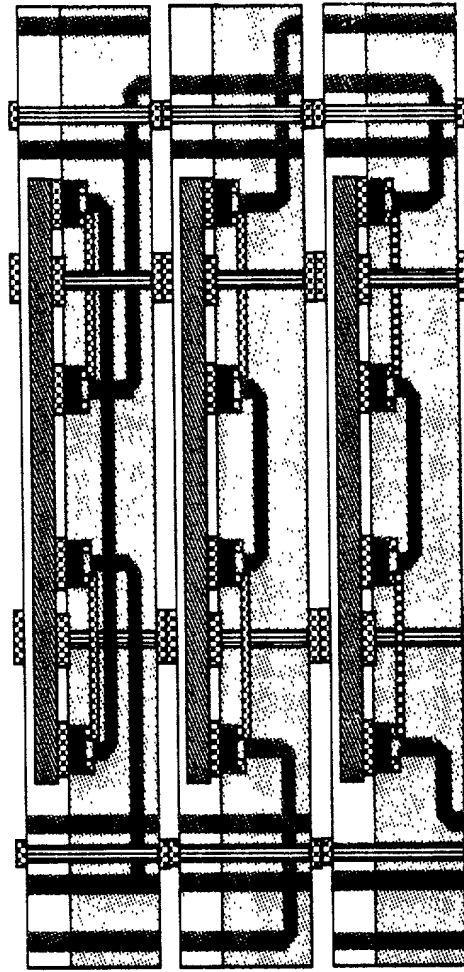
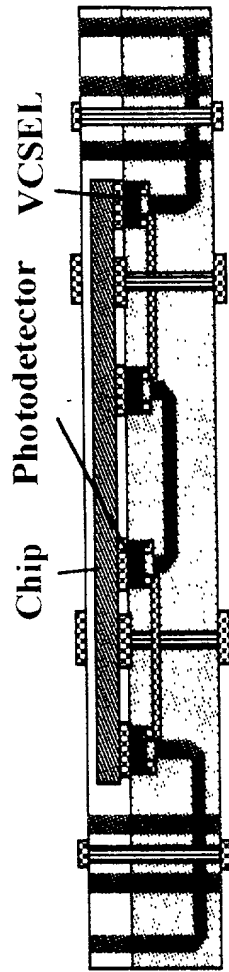


Fig. 110

A23

(2/23/99) AA1 Detail picture Example for 3D-stack'

(New version of the AA1 of 2/5/99)

Figure 12-2'

A23 3/7/99

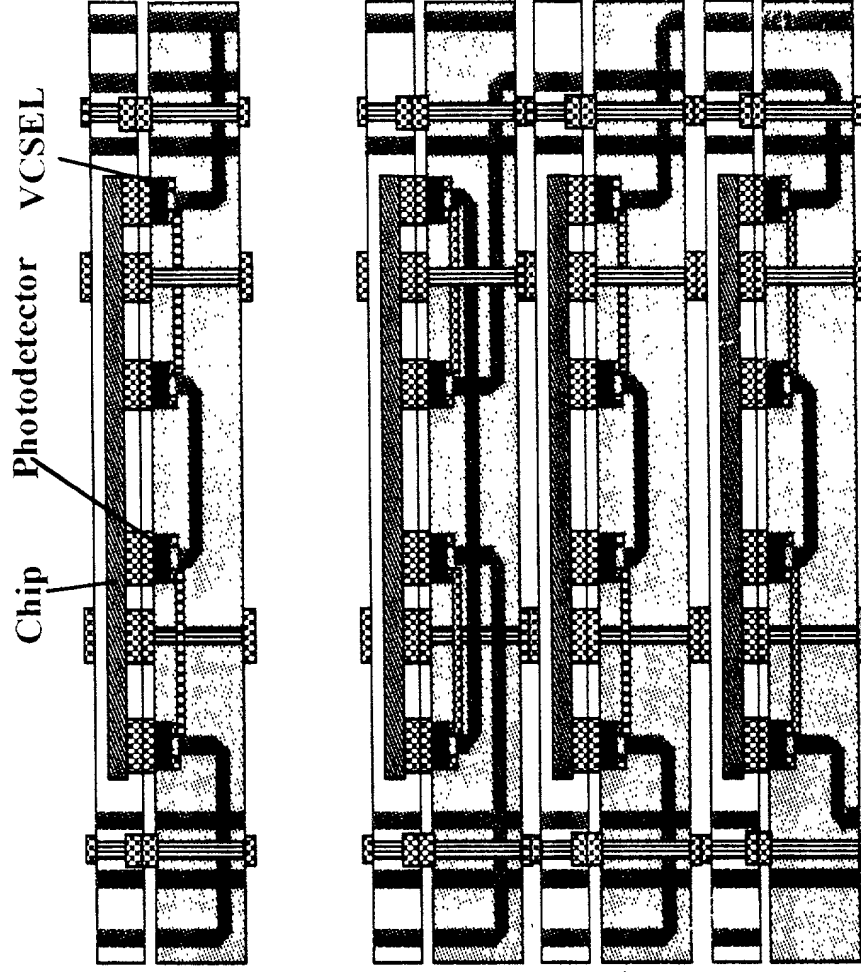


Fig. 110

A24

(2/23/99) AA2 Detail picture Example for 3D-stack'

(New version of the AA2 of 2/5/99)

A24 3/7/99

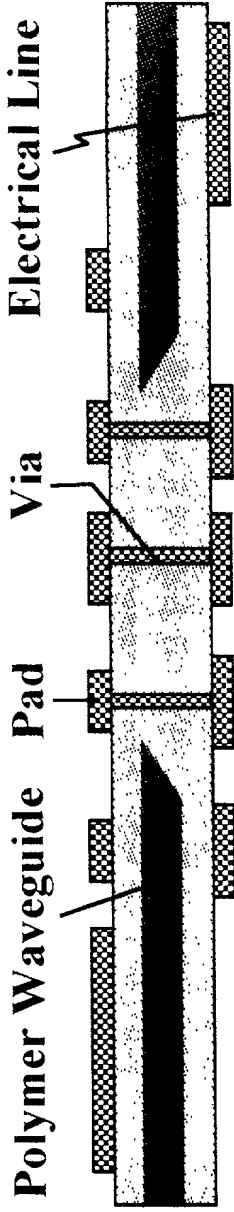
Figure 12-3'

720

Fig. 1/2

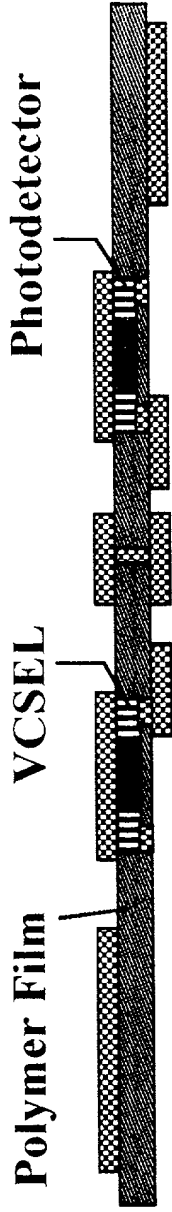
A 7 3/12/99

## OE-Films



OE-film-W

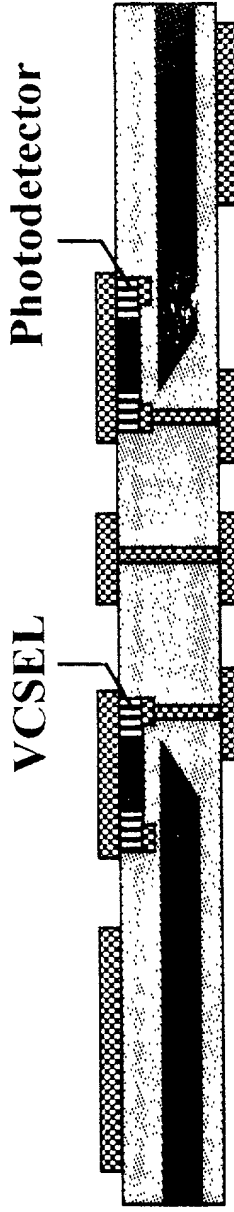
F16.113



OE-film-D

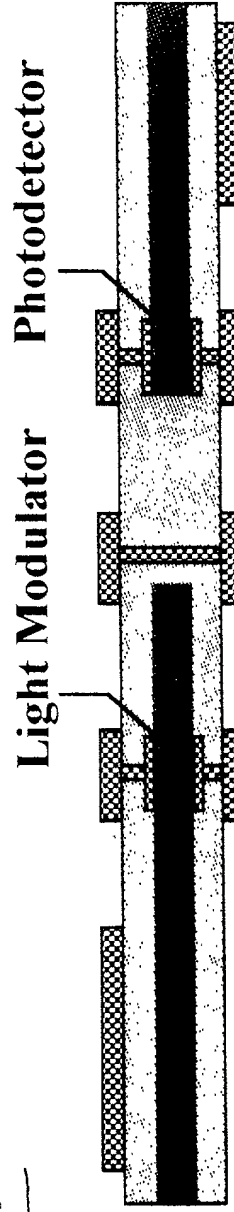
F16.114

A8



OE-film-DW(V)

F16.115



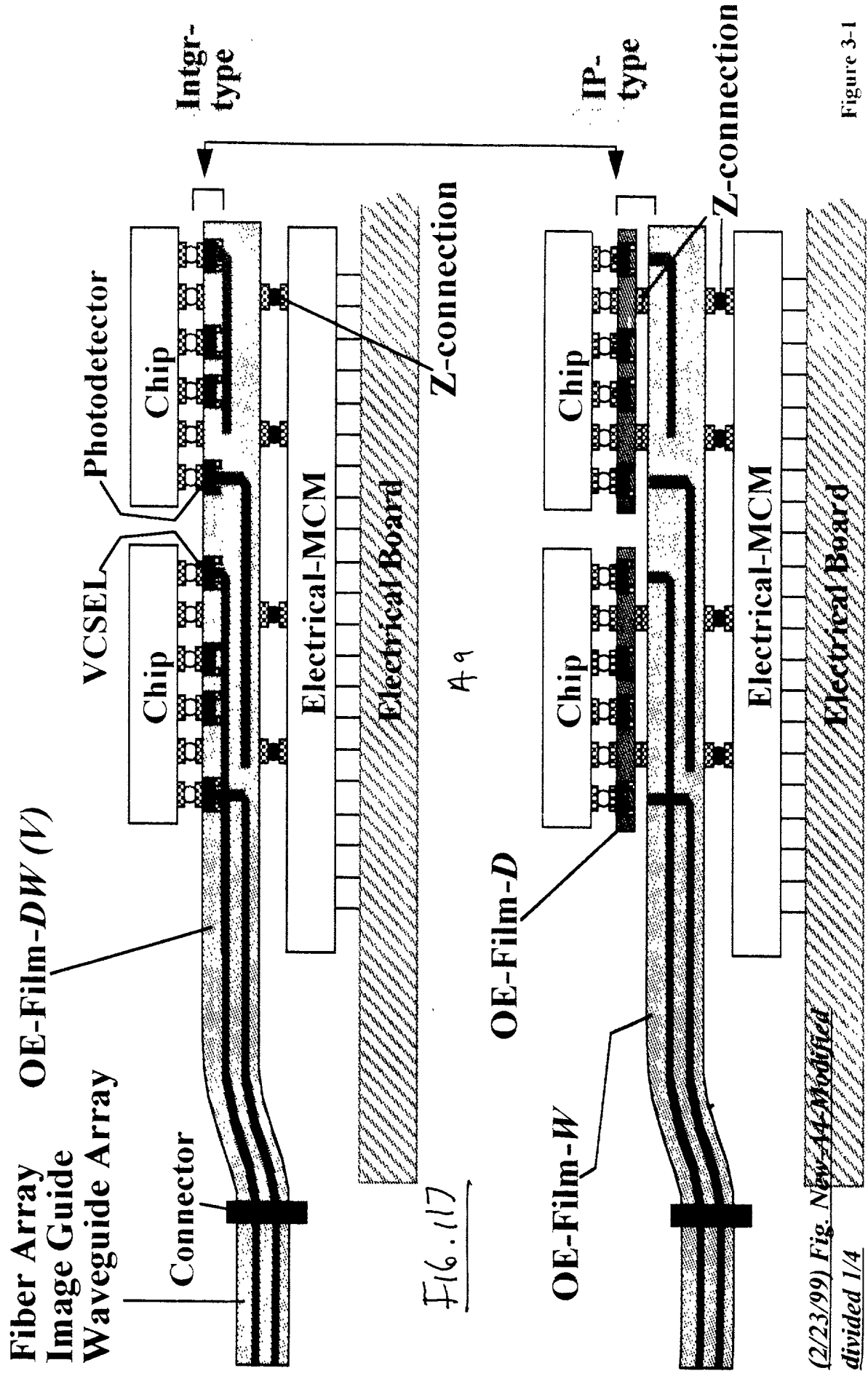
OE-film-DW(M)

2/17/99-added 2

F16.116

A8 3/27/99

# FOLM



F16.117

(2/23/99) Fig. New-A4-Modified divided 1/4

Figure 3-1

F16.118  
A9 3/27/99

A9

# FOLM

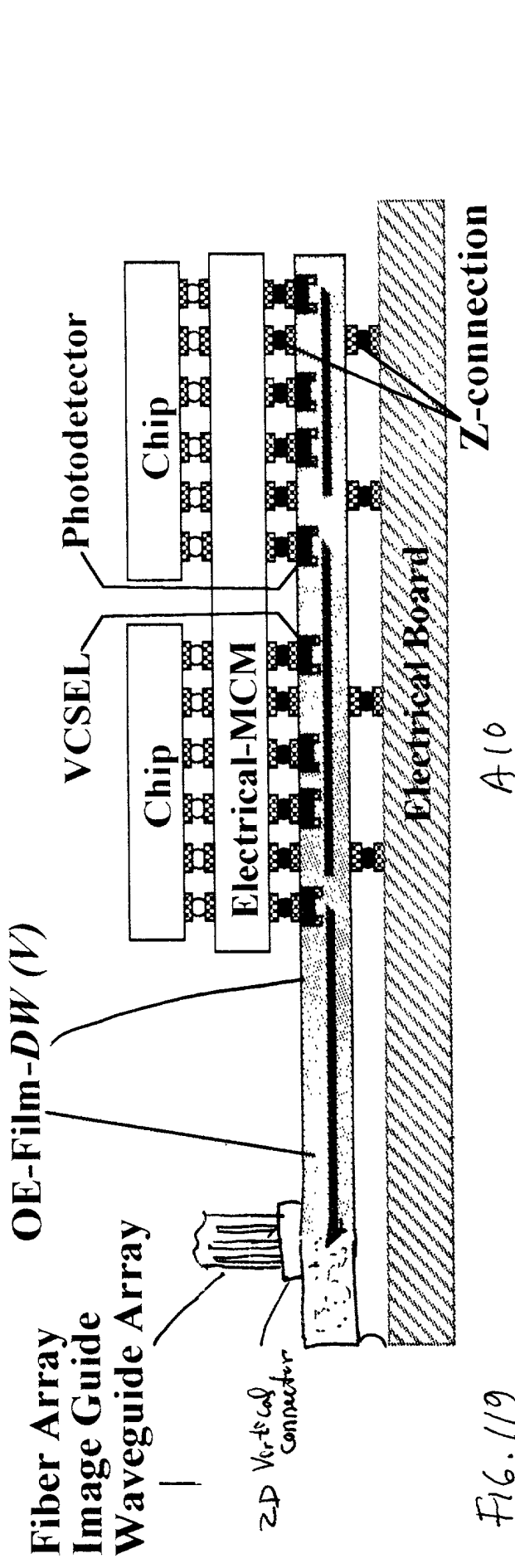
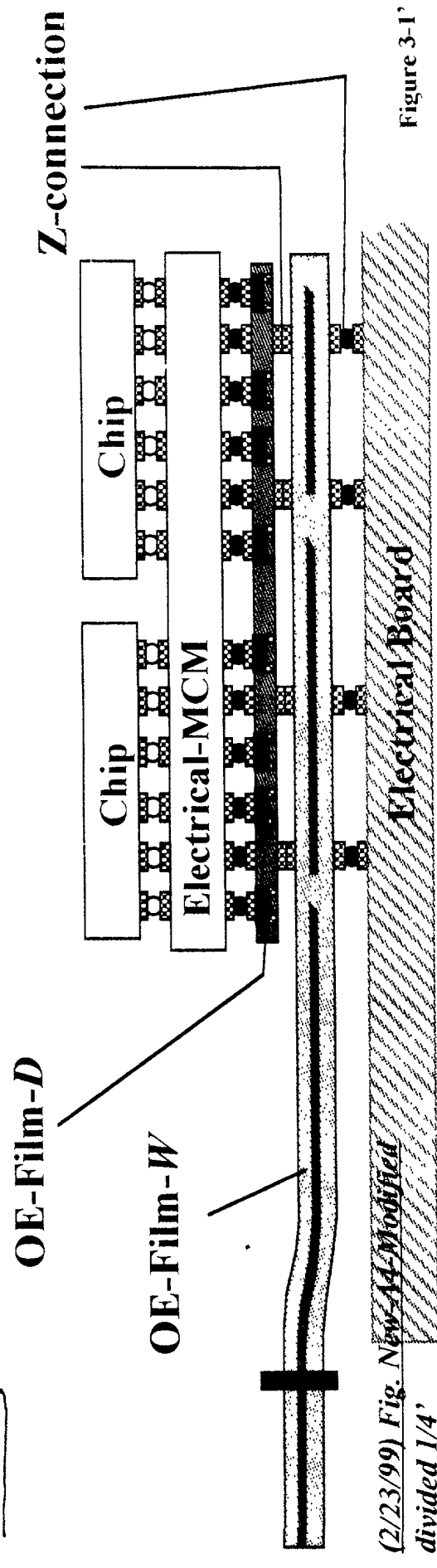


Fig. 119



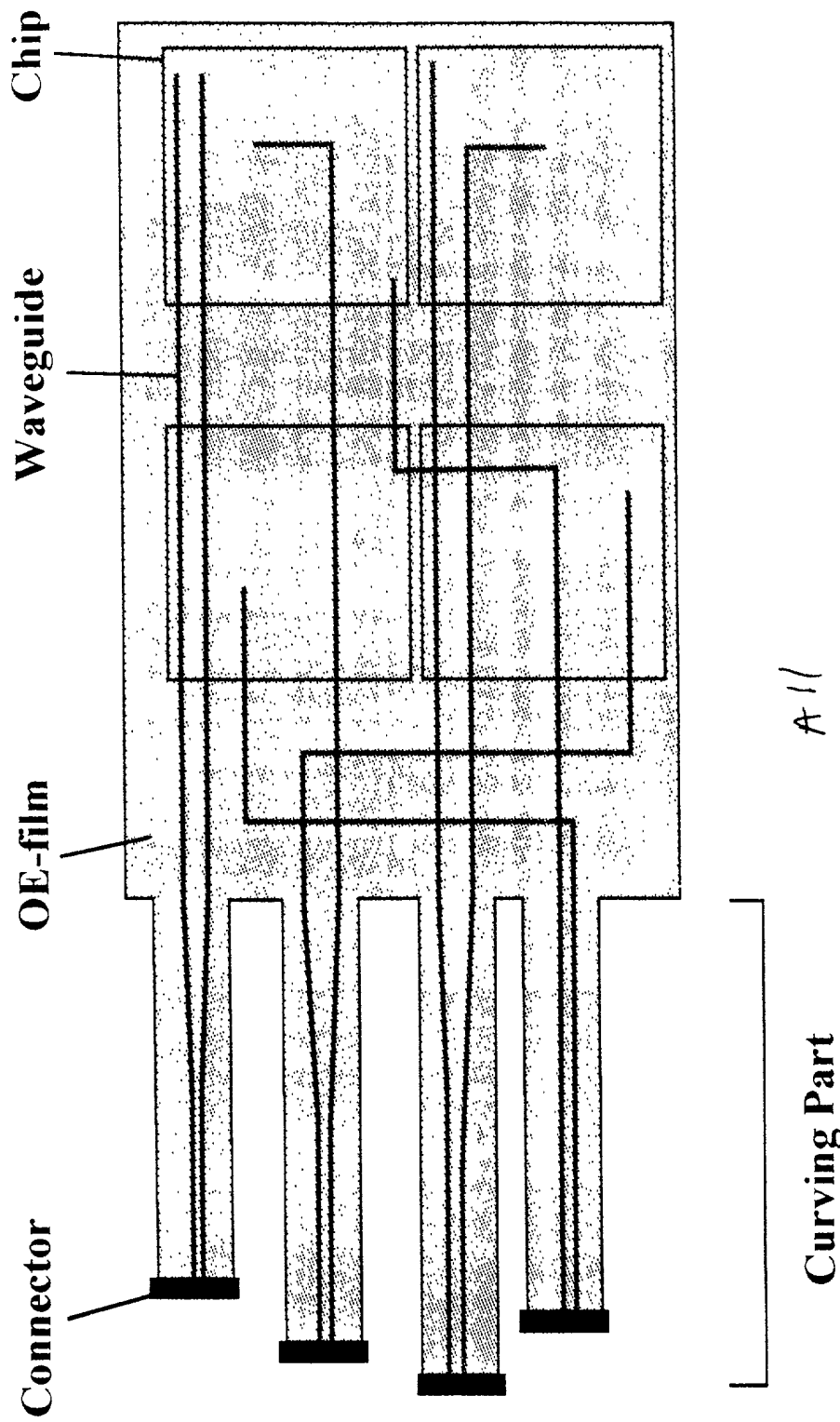
(2/23/99) Fig. New-A4 Modified divided 1/4'

Figure 3-1'

Fig. 120

A10 3/27/99

A10



Curving Part

A11

Fig. 121

(2/17/99) Fig. New-A4-Modified  
 divided 2/4

Figure 3-2

A11 3/2/99

111



**FUJITSU Computer Packaging Technologies, Inc. FCPT**  
**FOLM with Optical Path Length Controller, Connector Buffer**

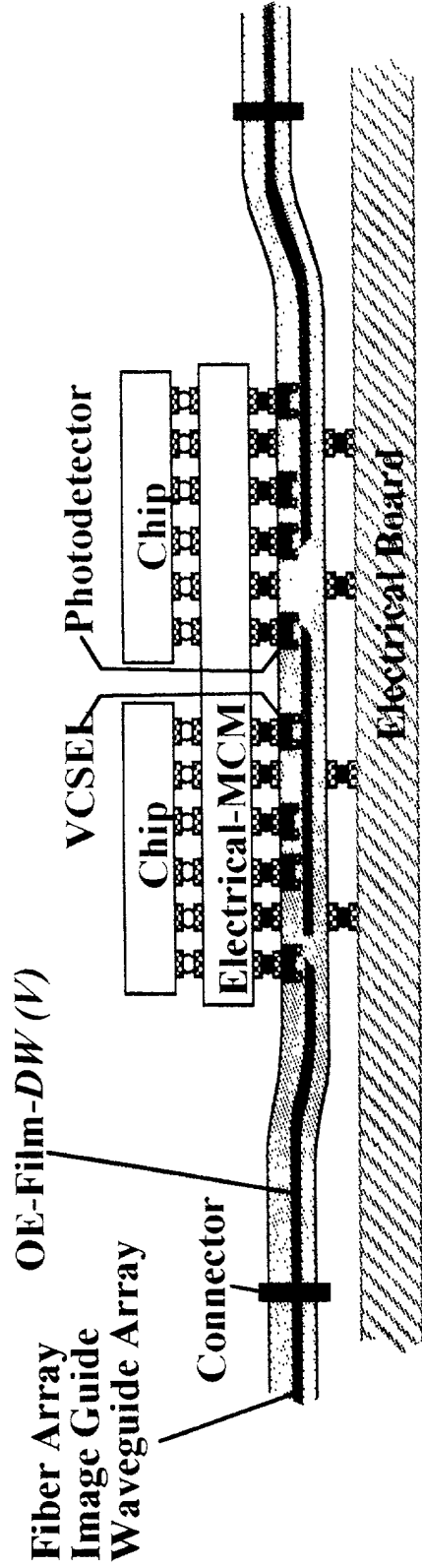


Fig. 123

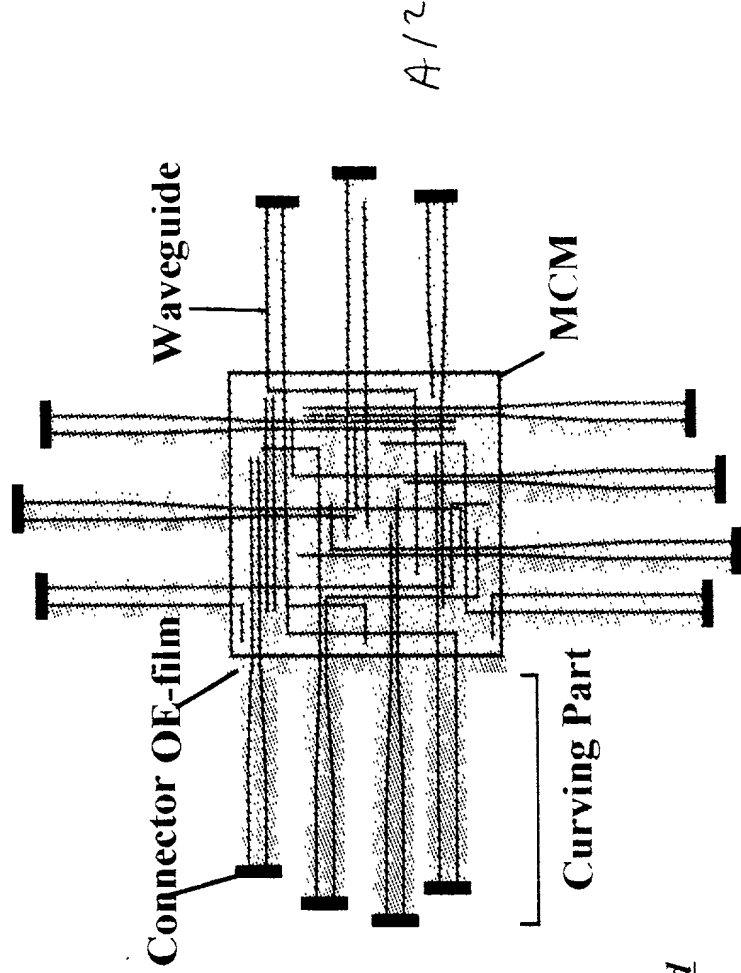
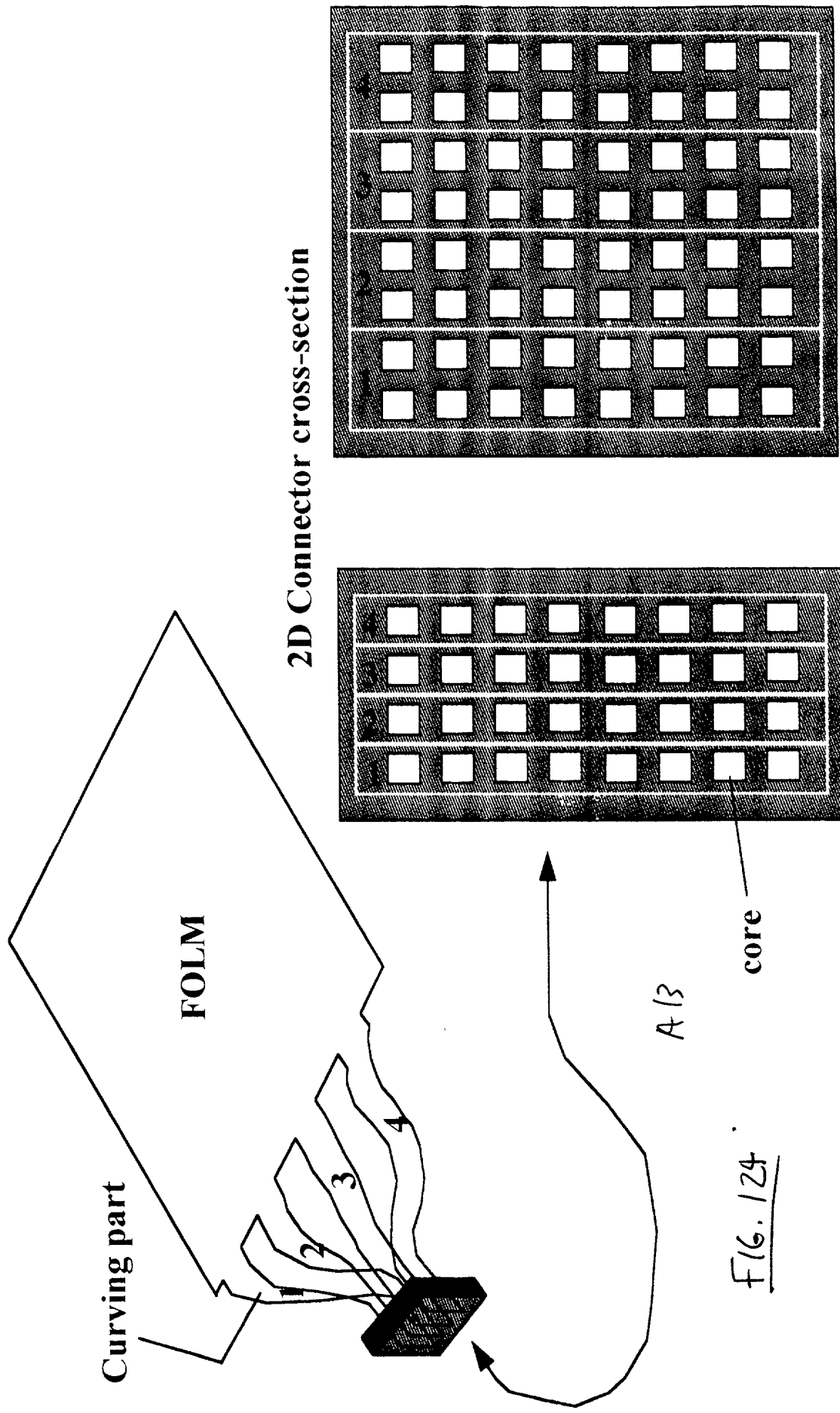


Fig. 122

(2/23/99) Fig. New-A4-Modified  
 divided 2/4'

Figure 3-2'

A12 3/7/99



(2/23/99) Fig. New-A4-Modified divided 3/4' (for Single-layer waveguide) (for 2-layer waveguide) Figure 3-3'

## FOLM: High-Speed Option

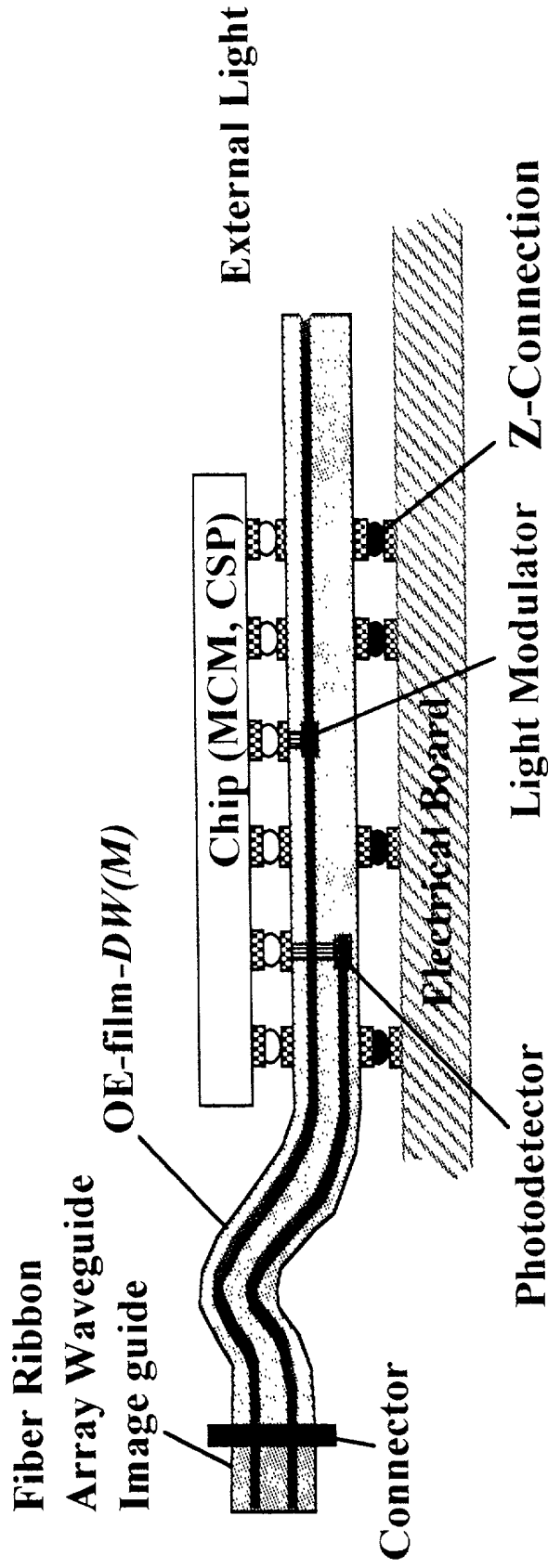


Fig. 125

A14

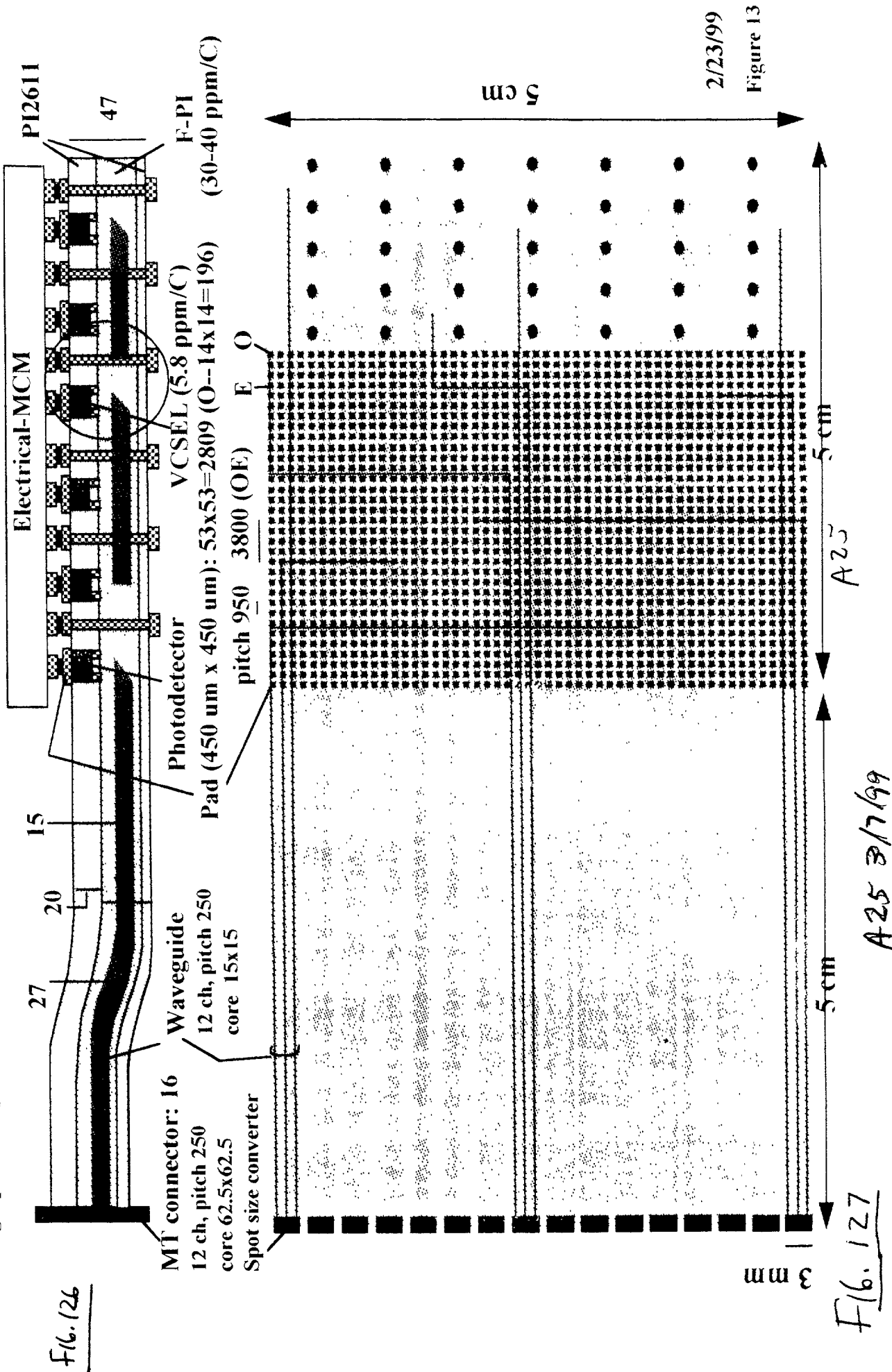
(2/17/99) Fig. New-A4-Modified  
divided 4/4

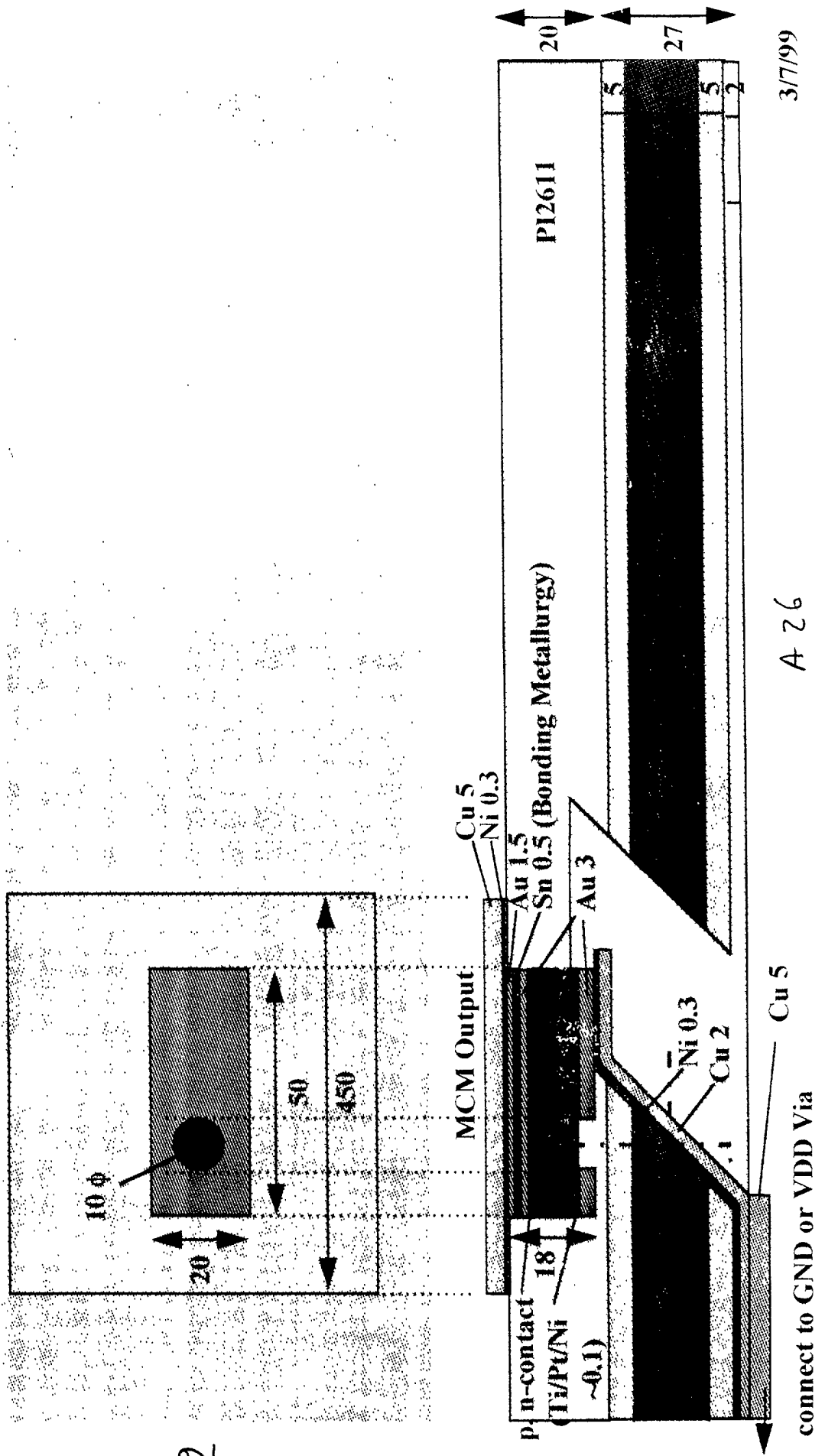
A14 3/7/99

# FOLM Structure Example (Overall)

Through put: 1.5 pbs x 196 ch Assume SSX MCM Size is ~5 cm x 5 cm

Unit: um





Unit : um

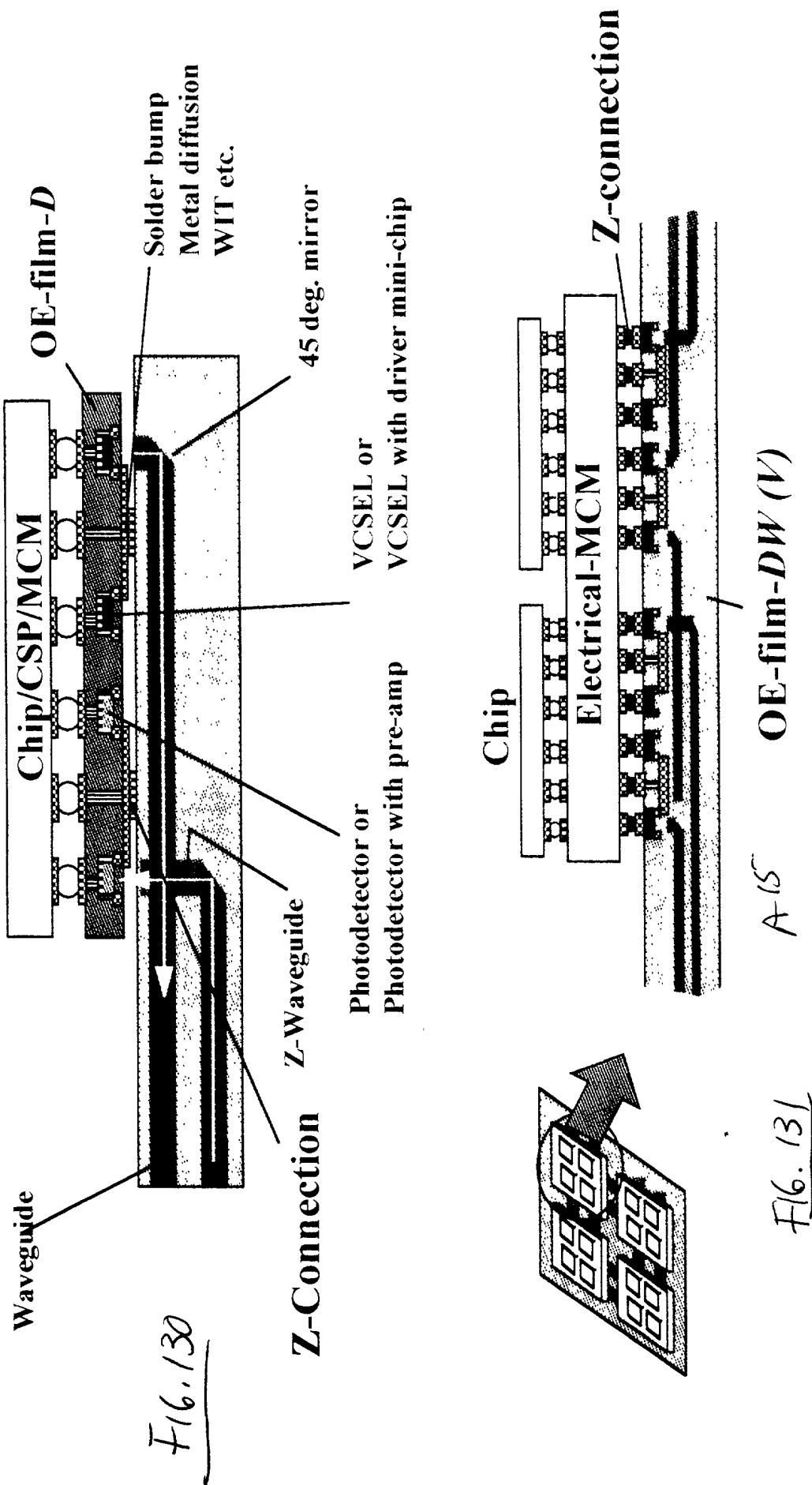
Fig. 128

Figure 14

A26 3/7/99

1A77

# **OE-film: OE-IP, OE-Film-MCM**



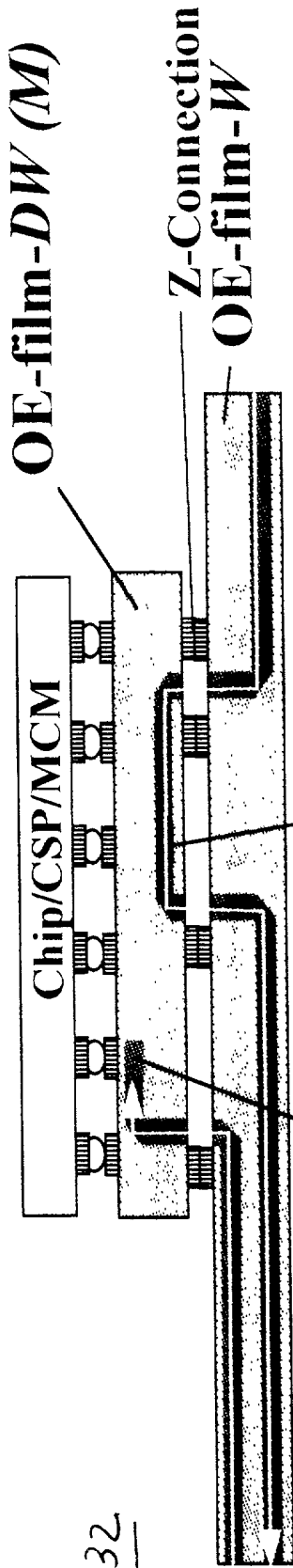
(2/23/99) Fig. New-A1-Modified'

Figure 5'

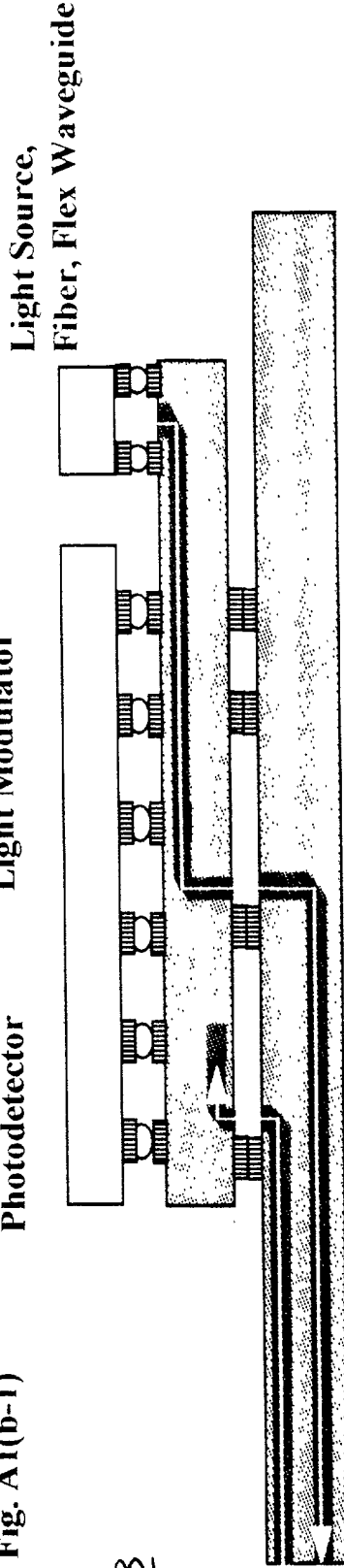
A15 3/7/99 [A15]

F16.131

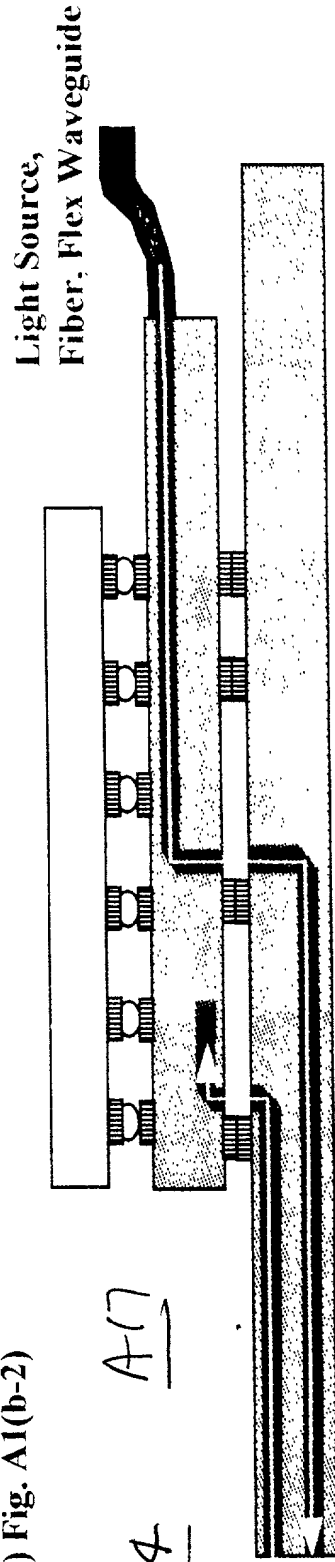
# OE-film: Light Modulator Transmitters



(2/17/99) Fig. A1(b-1)



(2/17/99) Fig. A1(b-2)



(2/23/99) Fig. A1(b-3)

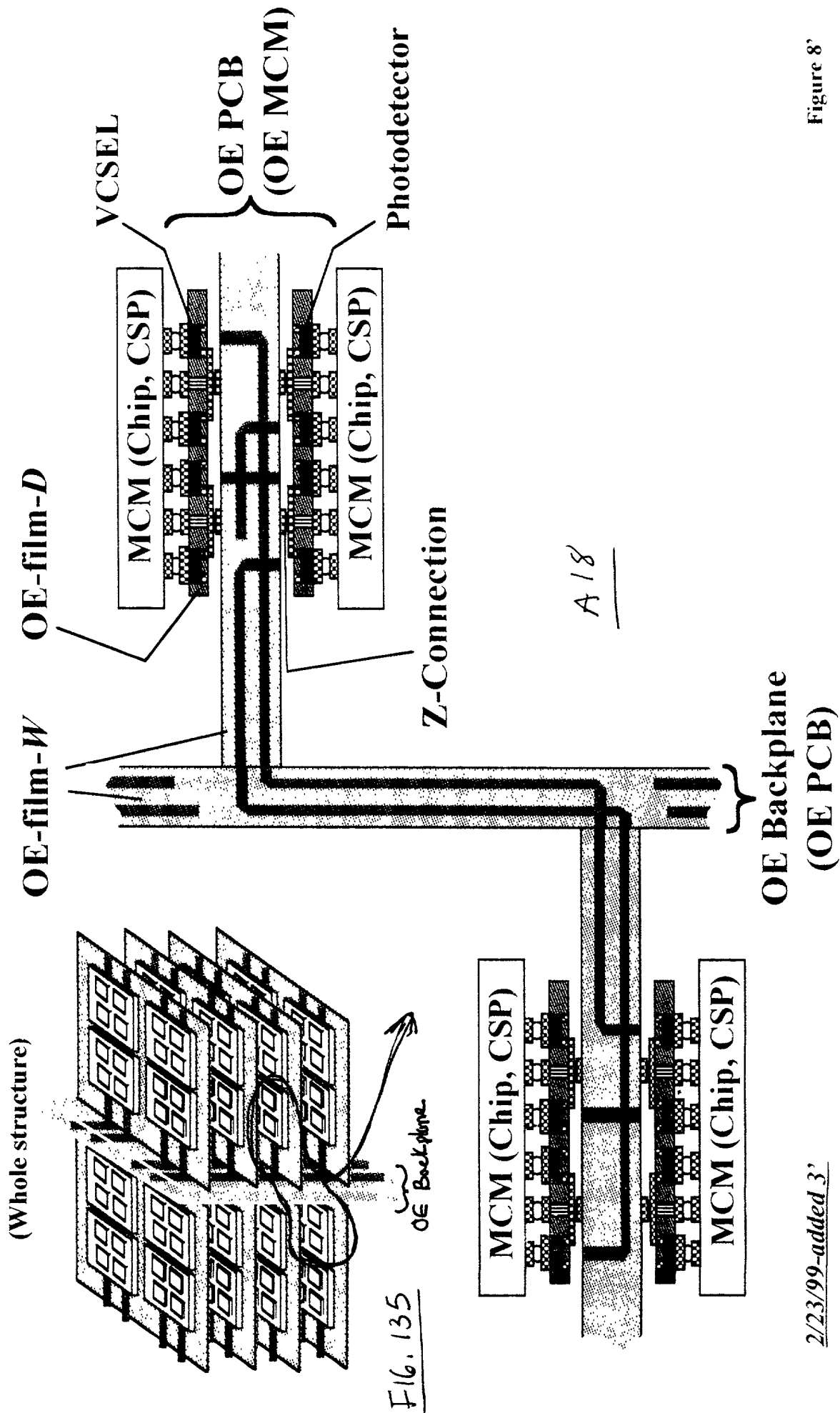
Examples of Light Modulators: Electro-Optic (EO) Modulator, Electro-Absorption (EA) Modulator

Figure 7

A17 3/7/99

A17

# OE-film: Both-Side Packaging



2/23/99-added 3'

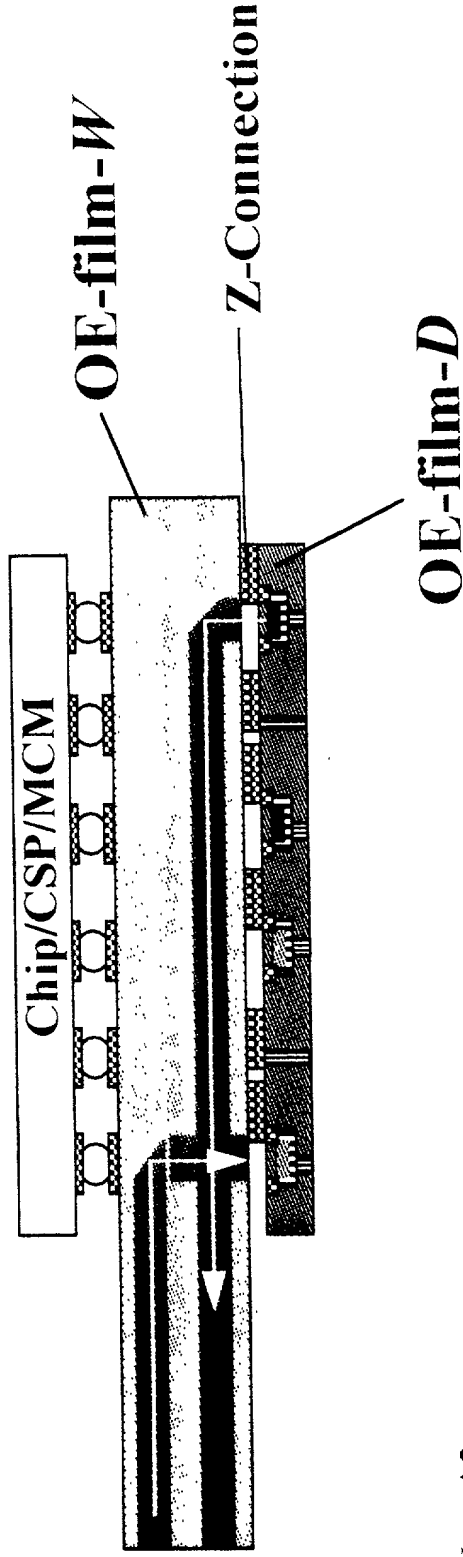
Figure 8'

A18 3/7/99

A18



# OE IP is Placed on the Oposit Side



(2/23/99) Fig. New-A2

F/6.138

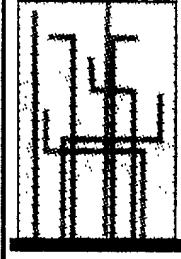
A20

Figure 10

A20 3/7/99

A20

# Direct Jump from LSI



Can act as  
Line length controller

## Fiber Ribbon Film Waveguide with Device Integration

Fig. 136

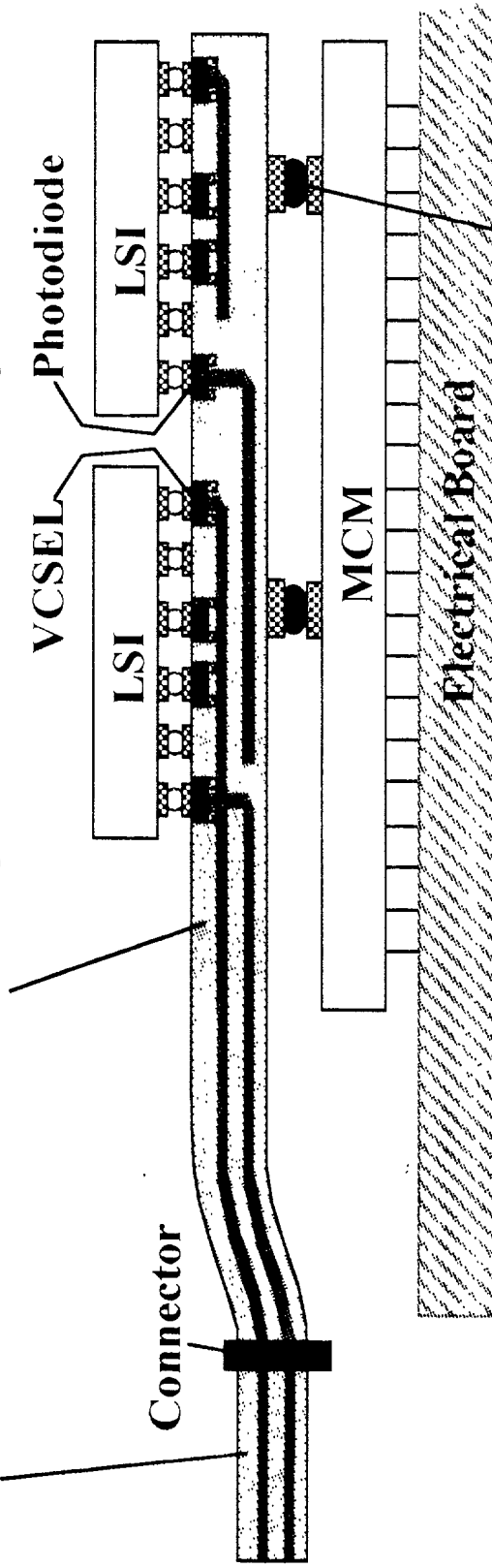


Fig. 137

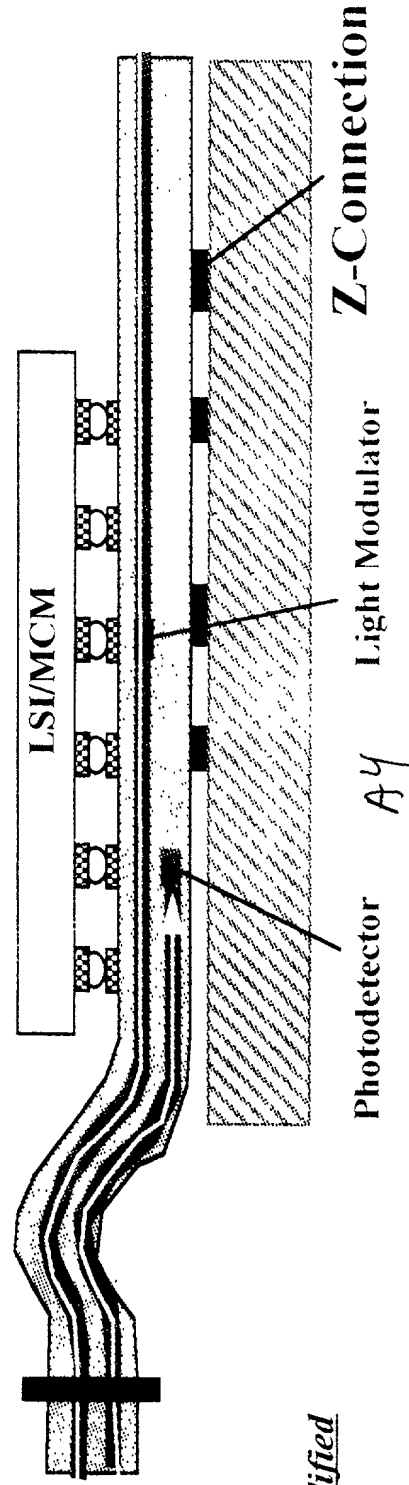
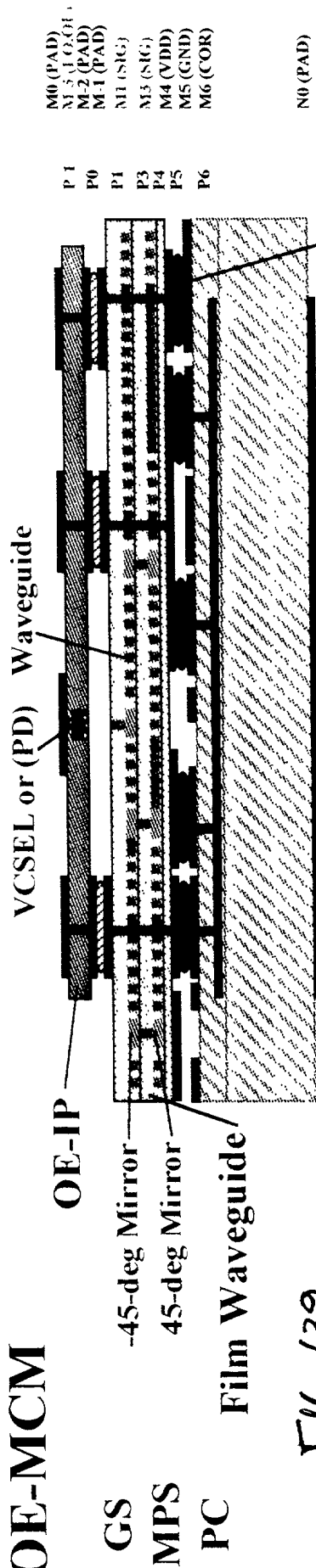


Fig. New-A4-Modified

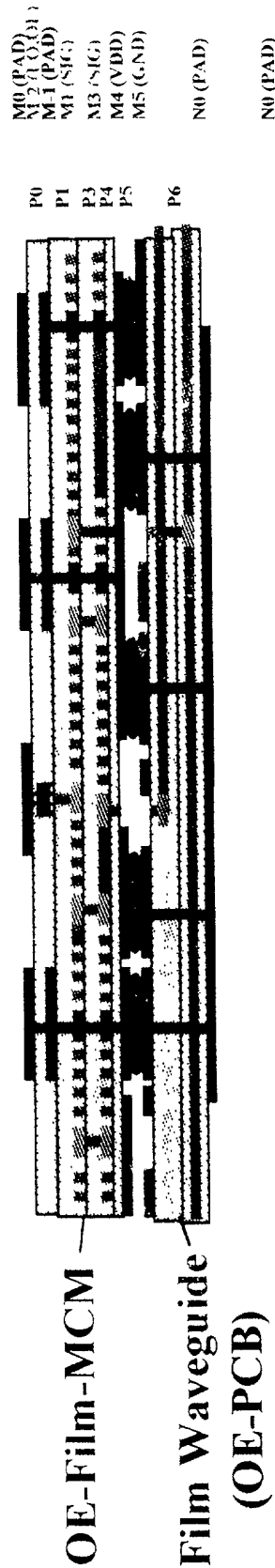
A4 1/18/99

**OE MCM**

**OE-MCM**



F16.139



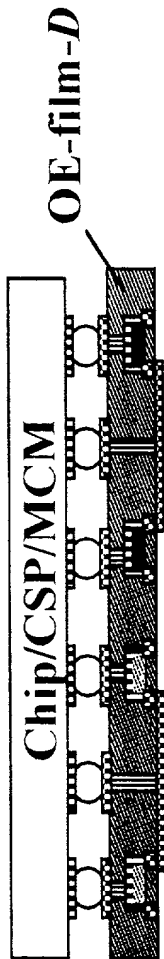
F16.140

A5

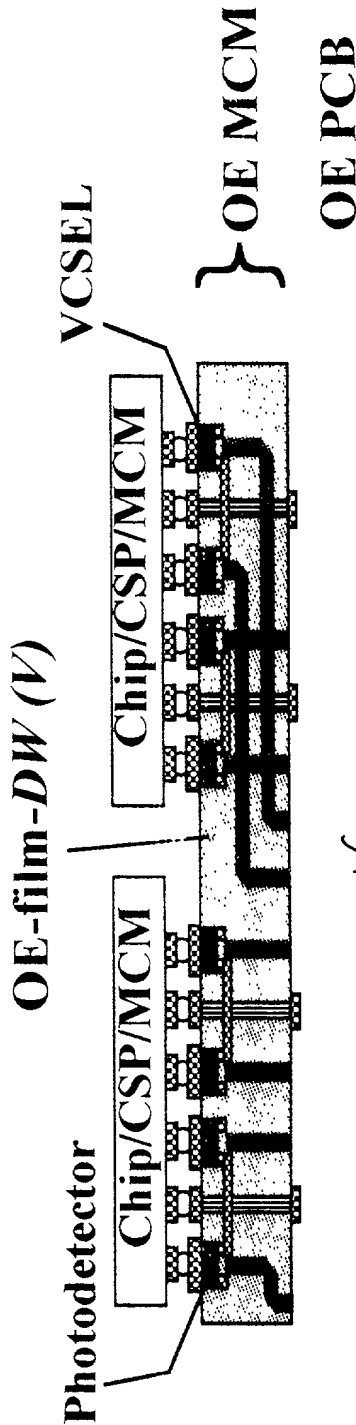
Fig. A5-Modifieg

A-5 11/18/99

## OE-film: Smart Pixel



F16.141



F16.142

A16

2/23/99-added 6'

Figure 6'

A16 3/7/99

OE-Film/OE-Film Stack --- Back-Side Connection

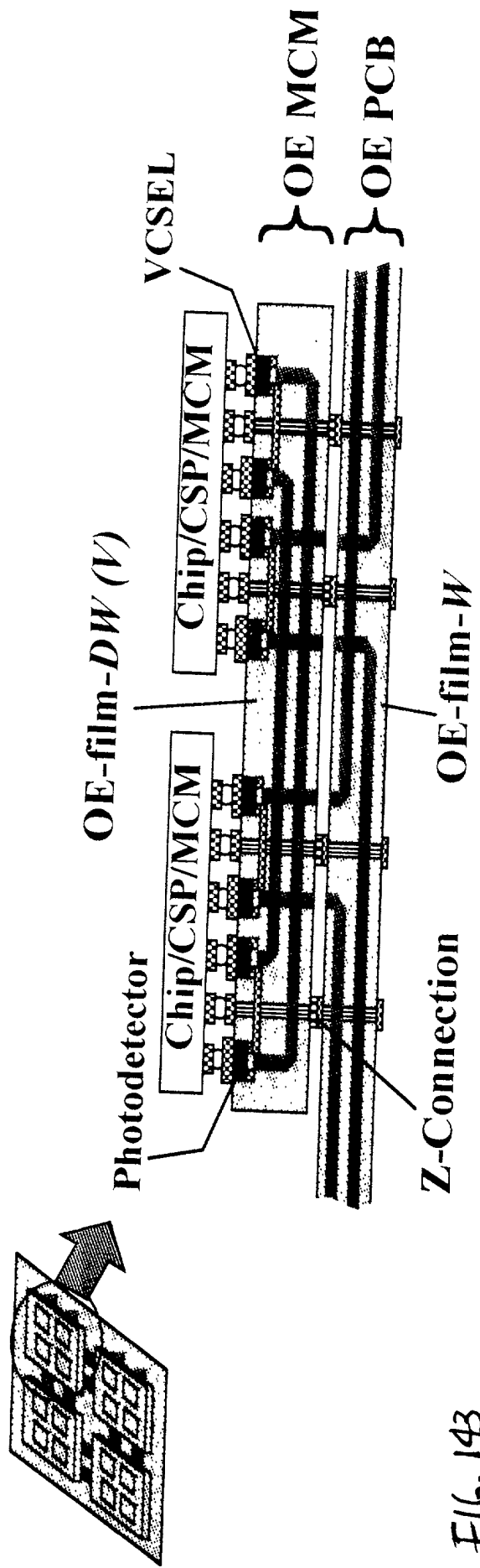


FIG. 143

A19

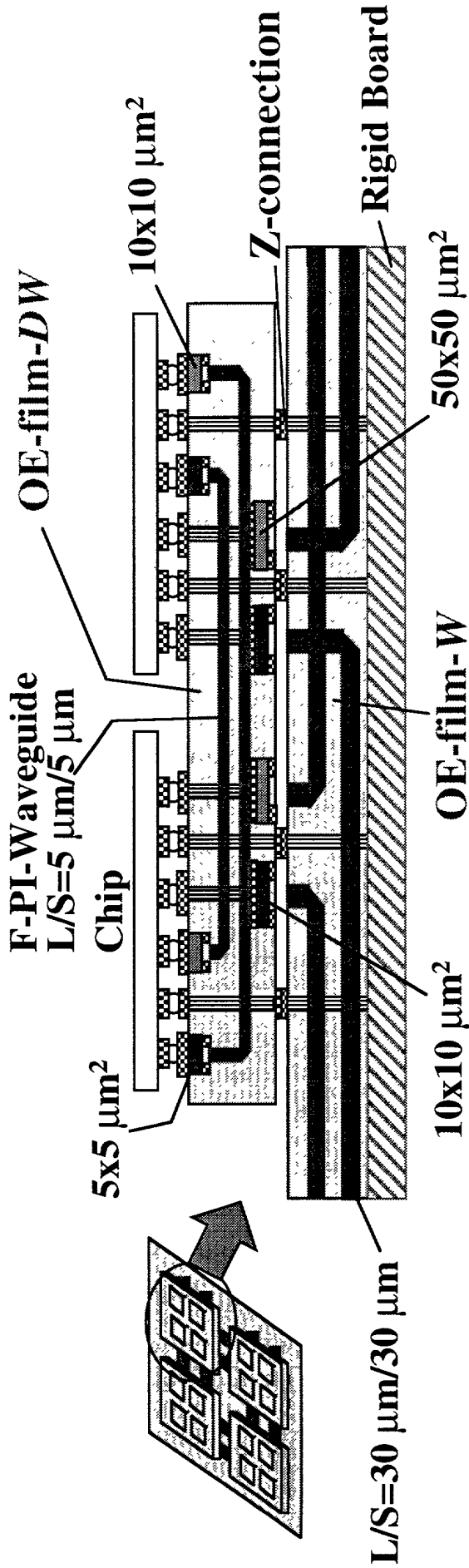
2/23/99-added 4'

Figure 9'

A19 3/7/99

A19

# OE-Film/OE-Film Stack --- Back-Side Connection



DI

FIG. 144

Fig. 3/18/99-1

DI 3/18/99

3/4

# OE-MCM/OE-Bord Stack

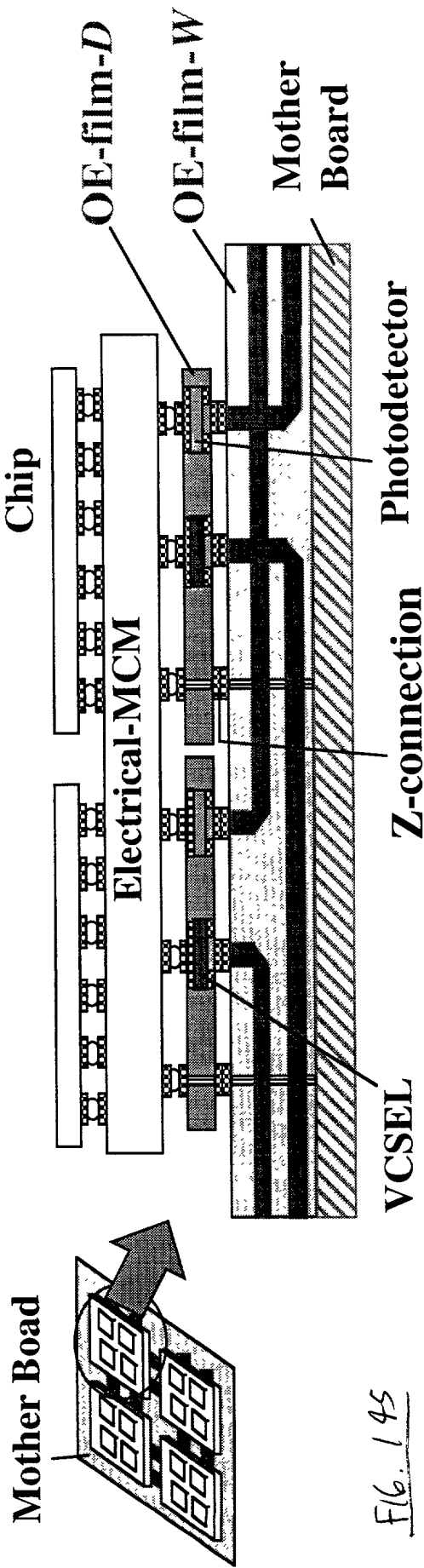


Fig. 145

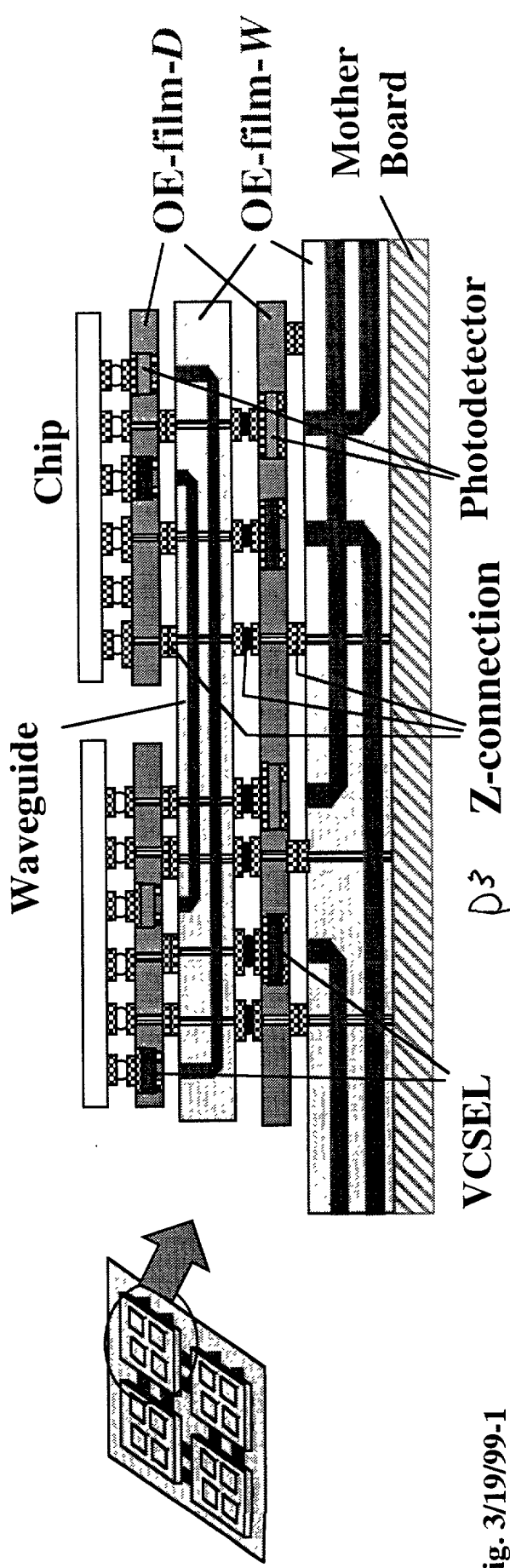
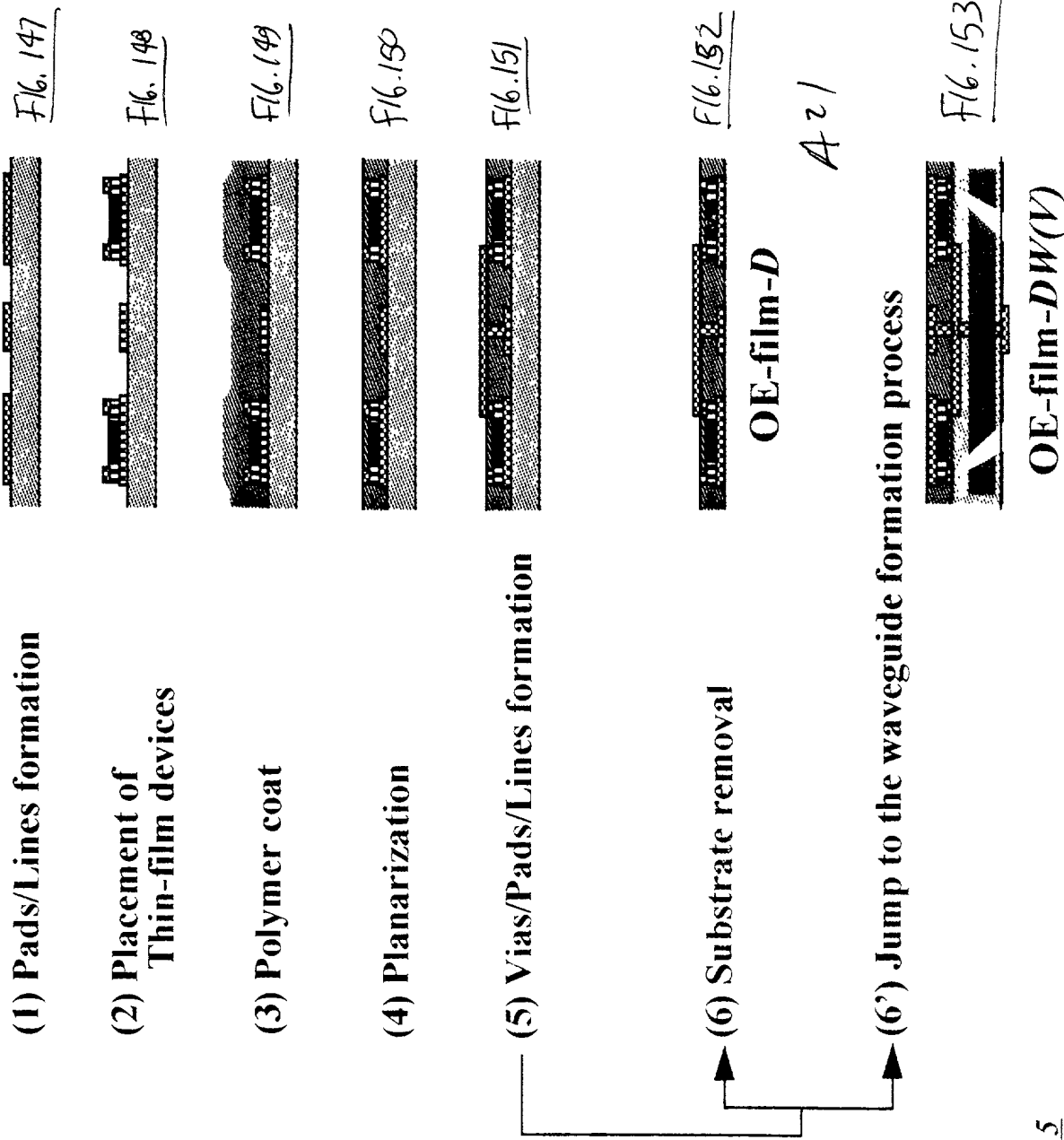


Fig. 3/19/99-1

Fig. 146

03 3/18/99

## Device Integration Process



2/17/99-added 5